457041

MODEL 8154

TIME CODE GENERATOR/READER/ TAPE SEARCH AND CONTROL UNIT OPERATING AND SERVICE MANUAL

SERIAL NO. 1383

AUSTRON

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REVISION G

NOTICE:

DISREGARD ALL SYSTRON DONNER

ADDRESSES AND TELEPHONE NUMBERS

WARRANTY

AUSTRON, INC., of Austin, Texas, warrants, for one year after delivery, to the original purchaser of any product manufactured by AUSTRON, that same shall be free of defects in material and workmanship. Obligation under this warranty shall be limited to repair or replacement, at AUSTRON's discretion, of any product or part thereof which has been returned by the original purchaser with transportation prepaid, and upon examination by AUSTRON, is found to be defective. AUSTRON assumes no reponsibility for loss or damage to equipment being returned for repair or replacement under the terms of this warranty.

For this warranty to be effective, the purchaser agrees that the equipment will be properly installed and maintained. Equipment which, upon examination by AUSTRON, requires repair or replacement of parts thereof as a result of improper installation, misuse, unauthorized alterations or repairs, or user negligence, such repairs or replacement of parts thereof will be made at cost.

AUSTRON makes no representation or warranty of any kind, either expressed or implied, with respect to equipment operation and procedures. Any action that the user may take in reliance upon the operation or accuracy of this equipment shall be taken solely upon the user's own responsibility and risk.

AUSTRON shall not be liable for consequential damages to purchaser, user, or any others resulting from the possession or use of this equipment.

Prior to return of a product under terms of this warranty, AUSTRON, INC., Austin, Texas, is to be notified. Notification is to include the Model Number and Serial Number of the product and full details of the problem.

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STANDARD OPTIONS

Standard options installed in your unit are checked below. Circuit descriptions for these options are provided in Chapter 6. Special modifications, when included, are described in Chapter 7.

SERIAL NUMBER

OPTION	DESCRIPTION
☐ A12A	Slow Code, Type A
☐ A12B	Slow Code, Type B
☐ A16	Control Bit Insertion
☐ A19	Group Parallel BCD Outputs
☐ A21	Computer Read Command
☐ B14	Crystal Oscillator (±5 parts in 10^7)
☐ B17	Flywheel Oscillator
☐ C11	IRIG A (10 kHz) Code
☐ C12A	Binary Seconds (17 Bits in Code)
☐ C12B	Binary Seconds (TOD) Parallel Output
☐ C17	NASA 28-Bit (100 Hz) Code
☐ C18	NASA 36-Bit (1 kHz) Code
☐ C26	XR3 (250 Hz) Code
☐ C26A	XR3 (1 kHz) Code
☐ C31	IRIG G (100 kHz) Code
☐ C40	IRIG A,B,C (100 Hz), C (1 kHz), E (100 Hz), E (1 kHz) Switch Selectable
☐ C41	IRIG A,B Switch Selectable
☐ C47	XR3 (250 Hz/1 kHz) Switch Selectable
☐ C48	IRIG H (100 Hz)
☐ C48A	IRIG H (1 kHz)
☐ D12	Buffers, Positive Level
☐ D13	Buffers, Negative Level
☐ D14	Buffer Storage
☐ D15	Parallel BCD Output (TOD)
☐ D15A	Parallel BCD Output (Days/ID)
☐ E13	Days/ID Number (Generate, Read and Search)
☐ E14	Milliseconds

	OPTION	DESCRIPTION
☐	E14A	Parallel BCD Output (Milliseconds)
☐	E19	Selectable Search
☒	L12	48 Hz to 440 Hz Operation
☐	L13	AC/DC Power Supply
☐	P11	Remote Mode Control
☐	P14	Remote Code Select (Option C40)
☐	P20	Remote Slow Code Rate Select
☐	S11	External Synchronization
☐	S11A	WWV Synchronization
☐	S13	Analog Filters
☐	S14	Analog Filters with Remote Select
☐		Special Modifications (See Chapter 7)

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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 8154 Time Code Generator/Reader/Tape Search and Control Unit combines functions normally provided in separate units.

As a Time Code Generator, the Model 8154 is a precise digital clock which displays time and generates a serial time code. This time code may be used in many applications where real or elapsed time must be maintained for control, recording or display. In the case of the Model 8154, however, its main use is for recording continuous time (to index data) on magnetic tape.

As a Time Code Reader, the Model 8154 decodes an incoming serial modulated time code during data playback. Time information stripped from the input code is displayed and fed in parallel BCD form to the Tape Search section. The Reader incorporates extended range AGC, error bypass, and digital filtering for reliable decoding of the incoming time code.

As a Tape Search and Control Unit, the Reader is combined with the Tape Search section to form an automatic tape search system. The Tape Search section operates essentially as a limit comparator which compares the decoded tape time from the Reader with selected Start and Stop times programmed on front panel thumbwheel switches. Manual override and search capability is provided in addition to the automatic modes.

During automatic search operation a programmed search sequence may be initiated by selecting *either* the forward or reverse tape direction. If the wrong direction is chosen, the Model 8154 automatically reverses the transport, driving it in the proper direction required to locate the preselected Start time. This is made possible by the full "high-low" comparator used in the Tape Search section. The comparator logic makes a decision *each* time-frame to determine if the tape time is *less than* or *greater than* the programmed Start (or Stop) time. As a result the possibility of missing coincidence, due to tape signal dropout or a garbled time-frame, is greatly reduced.

Status Indicators (front panel lamps) are provided which indicate whether the incoming tape time is *greater than* or *less than* the programmed start time and when the transport is in Drive and tape time is in the Interval between the Start and Stop times. A relay assembly is provided to control the tape transport through transfer contacts accessible through a rear panel connector. (Representative interface information is presented in the Appendix.)

The basic unit generates or reads a modified IRIG B time code on a 1 kHz carrier. Time is displayed in hours, minutes and seconds. Front

panel thumbwheel switches are provided for entering Generator preset (Start) time or Tape Search section Start and Stop times in hours, minutes and seconds. Four pulse rates (1 pps, 10 pps, 100 pps and 1 kpps) are supplied as outputs.

Other time codes from the IRIG, NASA and XR3 code families may be substituted for IRIG B as options. The unit can be expanded to include Days/ID Number and to provide parallel BCD outputs representing Days/ID through Milliseconds. Other options are also available (refer to the standard option list at the front of this manual).

The Model 8154 is constructed with highly reliable semiconductors and monolithic IC's assembled on printed-circuit, plug-in modules for ease of maintenance.

1.2 SPECIFICATIONS

1.2.1 Time Base (Generate Mode)

Crystal-controlled oscillator with an aging rate of 1 part in 10^7 per day and an overall stability of 1 part in 10^5 per day from 0° to 60°C. Provisions are included for the use of an external 1 MHz time base.

1.2.2 Display (Generate and Read/Search Modes)

A 6-digit, in-line, in-plane display indicates time-of-day in hours, minutes and seconds. Days option adds 3-digits. Numeral height is 0.55"(14 mm). Colons are provided between seconds and minutes, minutes and hours, and hours and days.

1.2.3 Code Format (Generate and Read/Search Modes)

Modified IRIG B format, in terms of BCD hours, minutes and seconds (Days/ID optional). Other IRIG, NASA or XR3 code formats are also available as options.

1.2.4 Inputs

1) External Time Base (Generate Mode): Accepts a 1 MHz (nominal) input at 1 V peak-to-peak (nominal) into 1 kΩ via a rear panel BNC connector. Selected by rear panel switch.

2) Elapsed Time Command (Generate Mode): A +5 V level (or open circuit) to enable, or a ground condition to inhibit time advance via rear panel connector, Amphenol 57-40360.

3) Update Inhibit (Generate or Read/Search Modes): A +5 V level (or open circuit) enables update. A ground condition delays update. Update may be delayed up to 0.5 ms without losing a count via rear panel connector, Amphenol 57-40360.

4) Modulated Code (Read/Search Modes): The input modulated code via a rear panel BNC connector may have a carrier frequency from 30 Hz to greater than 500 kHz. Input levels may be 50 mV to 50 V peak-to-peak with modulation ratios from 2:1 to 6:1. Input impedance is 100 kΩ minimum.

1.2.5 Outputs (Outputs are short-circuit-proof to ground)

1) Modulated Code (Generate Mode): The modulated code is generated on a 1 kHz carrier with an adjustable amplitude from 0 to 10 V peak-to-peak from a low impedance 15 mA source and an adjustable modulation ratio (Mark-to-Space) from 2:1 to 6:1. Connector is rear panel BNC type. The Code Format is modified IRIG B with BCD hours, minutes and seconds.

2) DC Level Shift Code (Generate and Read/Search Modes): The DC Level Shift Code is generated with an adjustable amplitude from 0 to 10 V into a minimum 600 Ω load. Connector is rear panel BNC type.

3) Pulse Rates (Generate and Read/Search Modes): Simultaneous rates of 1 pps, 10 pps, 100 pps and 1000 pps are provided with leading edge "on-time". Levels are 0 to +5 V(nominal). Connector is rear panel Amphenol 57-40360.

4) Status Signals (Automatic Search Modes): Separate Start and Stop pulse outputs (approximately 7 μs) are generated at Start and Stop times in Drive. In addition, complimentary Interval ($I/\overline{I}$) and Early Start outputs ($ES/\overline{ES}$) are provided. Levels are the same as for pulse rates.

5) Transport Control (Search Modes): Relay contacts accessible through rear panel connector. Contacts are rated 3 A at 30 V dc or 120 V ac (resistive load). Momentary (approximately 140 ms), or continuous (latched) Form C transfer commands are supplied as required by tape transport (See Appendix A).

The following commands are provided:

Forward (FWD) - High Speed
Reverse (REV) - High Speed
DRIVE or Playback - Drive Speed
Search Speed (SS)
STOP

1.2.6 Search Modes

1) Search to Start: Searches at high speed to the selected Start time; then, stops transport at least three time-frames in front of the Start time-frame.

2) Single Cycle: Searches to the selected Start time at high speed. Reproduces the selected tape segment at Drive (playback) speed; then, stops upon detection of the selected Stop time.

3) Recycle: Same as single cycle, except that upon reaching Stop time the system automatically searches for Start time again at high speed. The cycle is repeated until the STOP button is depressed.

4) Manual Search: Permits transport to be driven in the forward or reverse direction at a controlled speed. Model 8154 acts as a remote manual control for the transport.

1.2.7 Disconnect (Generate and Read Modes)

All control is returned to the tape transport in the Generate, Preset and Read Modes of operation of the Model 8154.

1.2.8 Start (Preset) and Stop Time Set

Two groups of thumbhweel switches for entry of Start and Stop times identifying a section of tape during search operation. The Start switches are also used for selecting the initial Start (Preset) time for the Generator.

1.2.9 General

1) Environment: 0°C to 50°C at up to 95% relative humidity.

2) Power: 115/230 V ±10%, 48 to 62 Hz at less than 60 W. (48 to 440 Hz operation is optional.)

3) Dimensions: 3 1/2" (8.9 cm) high by 19" (48.3 cm) wide by 17" (43.1 cm) deep. Removable rack flanges. Chassis drilled for Jonathan 120 QD series slides. Weight approximately 23 lbs (10.4 kg) net; 35 lbs (15.9 kg) shipping.

CHAPTER 2
INSTALLATION

2.1 INITIAL INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect it for damage. If any shipping damage is found refer to the warranty at the front of this manual and to Section 2.2 for repackaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your Systron-Donner representative.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185° F (85°C)

Minimum Temperature: -69° F (-55°C)

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.
2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb. sq. in. bursting strength) or wooden box to house the instrument.
3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.
4) Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".
5) Refer to the warranty at the front of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

2.3 POWER AND COOLING REQUIREMENTS

The Model 8154, unless otherwise specified, is supplied to operate from a 115 V ±10%, 48 to 62 Hz source.

To adapt the Model 8154 for 230 V operation, push the rear panel 115/230 V selector switch, S101, to the "230" position and change Fuse, F1, from 2 A slo-blo to 1 A slo-blo.

2.4 INITIAL ADJUSTMENT

To apply primary power to the Model 8154, it is only necessary to rotate the MODE switch to PWR OFF, install the power cord (supplied), and rotate the switch to GENerate.

2.4.1 Generator

The EXT-INT switch on the rear panel must be in the INT position to utilize the internal 1 MHz oscillator. If use of an external 1 MHz source is desired, the switch must be in the EXT position.

The Modulated Code Amplitude Adjustment Control on Card A8 (denoted as MOD) must be adjusted to the input voltage required by the particular tape transport in use (3 V peak-to-peak is standard). Voltage may be monitored at the CODE OUT BNC (J9) or at the MOD test point on A8.

The Modulation Ratio Control (marked as RATIO) has been factory adjusted for a 3:1 modulation ratio and should not require further adjustment. If adjustment should become necessary, the RATIO control on Card A8 may be adjusted as desired.

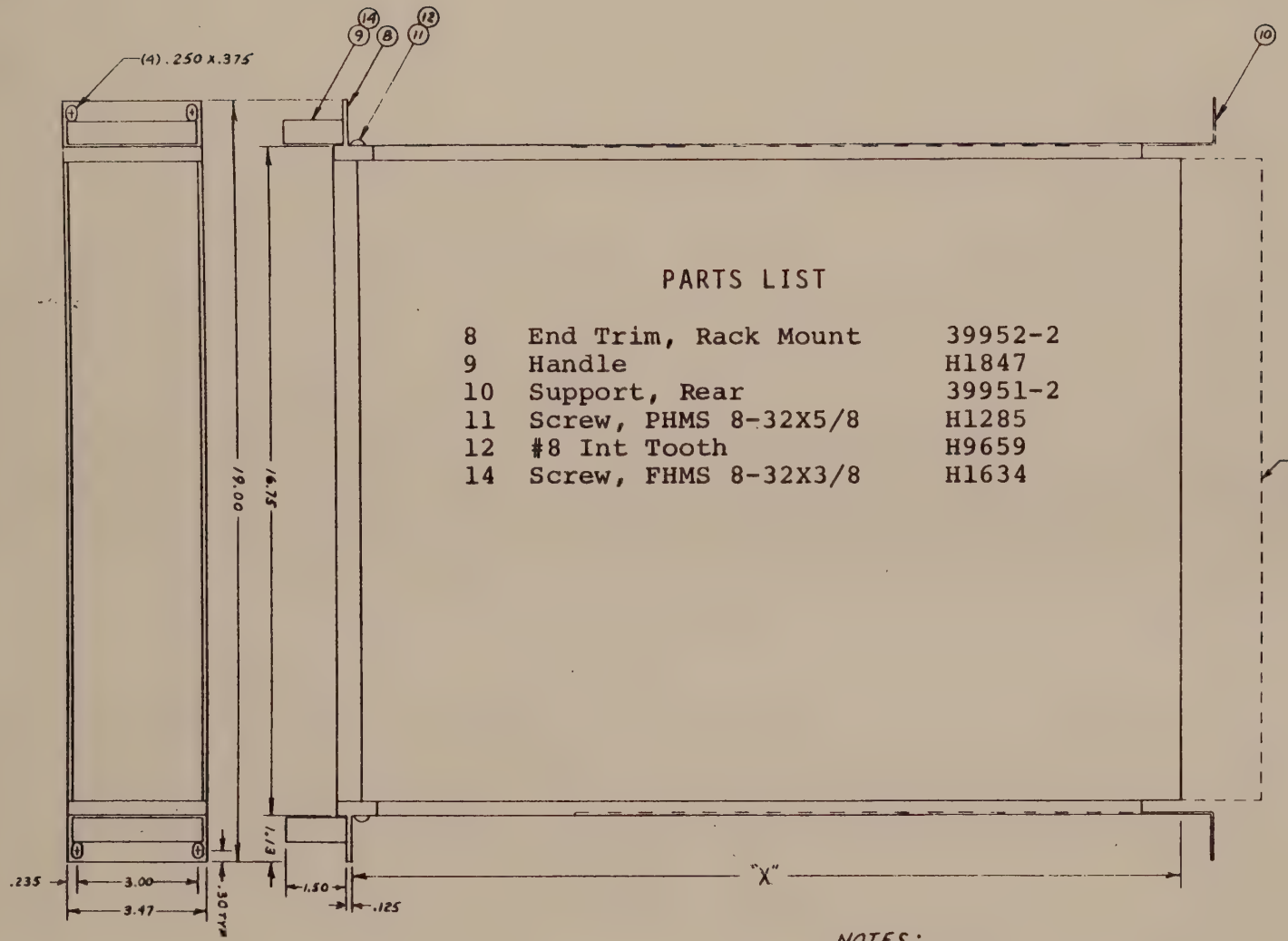
Also, if the Level Shift output is to be used, R19 on A8 (marked as DC) may be adjusted for the desired output level. R19 will adjust the Level Shift output from ground to +10 V dc. Monitor DC CODE (J10).

2.4.2 Reader

Turn the MODE switch to READ and introduce the appropriate code at J8. The unit should translate and display the time information contained in the code provided the input code is within specifications. No adjustment of the AGC (Card A10) should be necessary.

2.4.3 Tape Search and Control

Connect the unit to the tape transport to be controlled (See the Appendix for interface cabling. See Circuit Description for Relay Chassis Assembly #06137401 for relay programming information). Set the Stop Delay potentiometer (R3 on the rear panel) for a delay time which is longer than the longest time required for the transport to come to a complete stop from Fast Forward or Reverse.



PARTS LIST

8	End Trim, Rack Mount	39952-2
9	Handle	H1847
10	Support, Rear	39951-2
11	Screw, PHMS 8-32X5/8	H1285
12	#8 Int Tooth	H9659
14	Screw, FHMS 8-32X3/8	H1634

TABULATION

P/L #	"X"	W/STR. DEPTH
39986-1	8.75	9.12
39986-2	10.75	11.12
39986-3	12.75	13.12
39986-4	14.75	15.12
39986-5	16.75	17.12
39986-6	18.75	19.12
39986-7	20.75	21.12

NOTES:
1. INSTR. ARE DRILLED TO ACCEPT 20" JONATHAN 120 QD SERIES SLIDES
2. ITEM 10 DELETED WHEN SHIPPED W/SLIDES

FIGURE 2.1 3 1/2" FULL RACK ASSEMBLY #039986-5 REV A

2.5 INSTALLATION

The Model 8154 is normally supplied with hardware for rack-mount installation as shown in Figure 2.1.

For convenience, the unit has been drilled for 20" Jonathan 120 QD series slides. When slides are used, the rear support brackets (Item 10) are removed.

NOTE

Under no condition should air flow through the outlet hole in the rear of the unit be obstructed.

CHAPTER 3
OPERATION

3.1 GENERAL

The Model 8154 is ready to operate immediately after turning on the power. Preliminary adjustments or calibration (other than Stop Delay) are not normally required. It is advisable that the following description on use of the instrument controls and indicators be read before operating the unit.

3.2 CONTROLS, INDICATORS AND CONNECTORS

3.2.1 Front Panel

1) MODE Selector: (Rotary Switch S30) — Controls main power and selects mode of operation

   a) PWR OFF: — Removes power to the unit.

   b) PRESET: — Arms PRESET/RESET Switch and START (PRESET) Thumbwheel Switches. Stops time base counters and places Tape Search section in the Disconnect condition.

   c) GENerate: — Permits normal update of the display register and generation of the serial time code. Days/ID section of the PRESET/RESET circuit is armed (Days/ID Option), and the Tape Search section is in the Disconnect condition.

   d) READ: — Places the unit in the READ Mode of operation where time information is stripped from the input code and loaded into the display register. The Tape Search section is in the Disconnect condition.

   e) MANUAL: — Places the unit in READ Mode and converts the Tape Search section into a remote (Manual) control unit for the tape transport.

   f) TO START: — Places the unit in Read condition and selects an automatic mode in which the unit directs the tape transport to search for a preselected Start time at high speed. Stops transport at a point on tape ahead of the Start time. DRIVE (Playback) must be entered manually.

   g) SINGLE CYCLE: — Places the unit in Read condition and selects an automatic mode in which the Model 8154 directs the tape transport to search

for a preselected Start time at high speed then reproduce at Drive speed that section of tape between the Start time and a preselected Stop time.

h) RECYCLE: Same as SINGLE CYCLE except that the tape transport is directed to repeatedly reproduce the section of tape between the preselected Start and Stop times until manually commanded to Stop.

NOTE

When the MODE Switch is in the PWR OFF, PRESET, GENerate or READ position, the Tape Search section is in the "DISCONNECT" condition (all control is returned to the tape transport). When the MODE Switch is turned to the MANUAL, TO START, SINGLE CYCLE or RECYCLE position, the Tape Search section is activated in the "SEARCH" condition (tape transport is controlled by Model 8154) and the Reader/Generator section is in the Read Mode.

2) PRESET/RESET (Momentary Toggle Switch S31): Armed in PRESET position of the MODE Switch, Momentary PRESET loads the contents of the START (PRESET) thumbwheel switches into the display register. Momentary RESET forces display register contents to zero.

NOTE

If the Days/ID Option is included, the Days/ID section of the display register can be independently preset or reset in the GENerate position of the MODE switch.

3) START (PRESET): (Thumbwheel Switches S1-S6 TOD; S7-S9 Days/ ID Option): Used to enter Start (Preset) time information for loading into the Generator display register by the PRESET/RESET Switch in the PRESET position of the MODE Switch. (Days/ ID may also be entered in the GENerate Mode as described above.) Used to enter Start time for Search operation.

4) STOP: (Thumbwheel Switches S13-S18 TOD; S19-S21 Days/ ID Option): Used to enter Stop time for Search operation.

5) ERROR BYPASS: (Toggle Switch S40): If in the ON position when operating in READ or any of the Search Modes, the Reader section will ignore up to 3 consecutive frames with errors in forward.

6) FWD: (Lighted Momentary Pushbutton Switch S25): With the MODE Switch in READ, pressing the FWD pushbutton adapts the Reader to accept a forward code.

With the MODE Switch in the MANUAL position, pressing the FWD pushbutton initiates a fast forward movement of the tape which continues until manually stopped by pressing the STOP pushbutton.

With the MODE Switch in any of the 3 automatic Mode positions, pressing the FWD pushbutton initiates Search Forward. If the tape time is less than the preset Start time, Search Forward continues until the first frame greater than Start time. At this point it passes through an intermediate Stop condition; then, into Reverse. Upon detecting Start time in Reverse, it overshoots 3 successive frames; then, enters Stop. If the (Search) TO START Mode is selected, it remains in Stop. If set in SINGLE CYCLE or RECYCLE, it enters DRIVE and continues until Stop time at DRIVE speed. Upon detecting Stop time, it will Stop if in SINGLE CYCLE. If in RECYCLE, it continues on through Stop; goes into Fast Reverse back through Start time, then into DRIVE to repeat the cycle.

If the time on tape is greater than the Start time when the FWD pushbutton is pressed, the Model 8154 starts forward, detects greater than Start time; then, automatically enters Reverse after an intermediate Stop Delay. Subsequent operation is then as described above.

7) REV: (Lighted Momentary Pushbutton Switch S26)

With the MODE Switch in READ, pressing the REV pushbutton adapts the Reader to accept a reverse code. With the MODE Switch in the MANUAL position, pressing the REV pushbutton initiates a Fast Reverse movement of the tape which continues until manually stopped.

With the MODE Switch in any of the 3 automatic positions, pressing the REV pushbutton initiates Search Reverse. If tape time is greater than the preset Start time, Search Reverse continues to a tape time, 3 frames less than Start time. From here, the sequence is the same as described above.

If the tape time is less than Start time when the REV pushbutton is pressed, the Model 8154 starts in Reverse, detects less than Start time; then, enters Search Forward following the sequence above.

8) DRIVE: (Lighted Momentary Pushbutton Switch S27)

With the MODE Switch in the MANUAL position, pressing the DRIVE pushbutton places the transport in the Forward Drive (Playback) Mode, which continues until manually stopped.

With the MODE Switch in any of the 3 automatic Mode positions, pressing the DRIVE pushbutton initiates Forward Drive. If the tape time is greater than Start time, the Model 8154 will detect greater than Start time; then, Stop (Abort). If the tape time is less than Start time, it will continue in Drive until it detects Stop time. At this point it will enter Stop, if in SINGLE CYCLE or (Search) TO START. It will follow the sequence described above if in RECYCLE.

9) STOP: (Lighted Momentary Pushbutton Switch S29)

The STOP pushbutton is armed in all SEARCH positions of the MODE Switch. When the STOP pushbutton is pressed, the Model 8154 immediately goes to the Stop condition. It remains there until another operating condition is initiated manually.

10) Pushbutton Indicators: (DS25,DS26,DS27, and DS29)

Each of the 4 function pushbuttons (FWD,REV, DRIVE and STOP) is provided with a lamp which lights when the Model 8154 is in that Mode of operation.

11) "<" and ">": (Indicators DS6 and DS7)

The less than (<) and greater than (>) lamps indicate the relationship between tape time and the preset Start time.

12) INT Indicator: (DS8)

The INTerval lamp is lighted in DRIVE when the tape time is between the preset Start and Stop times and the MODE Switch is in one of the automatic Mode positions.

13) Display:

A 6-digit, in-line, planar readout which indicates TOD in hours, minutes and seconds. Days/ID Option adds 3-digits.

3.2.2 Rear Panel

1) BCD OUT (Optional): (50-pin Connector J3)

BCD Output of the display register contents. Option D15 provides TOD and Option D15A provides Days/ID.

2) Auxiliary: (50-pin Connector J5)

Reserved for options.

3) BCD MS: (14-pin Connector J6)

BCD Milliseconds outputs. Option E14A.

4)	PULSE RATES/REMOTE: (36-pin connector J7)	Pulse Rate outputs, status outputs and control inputs.
5)	CODE IN: (BNC Connector J8)	Code input to Reader
6)	CODE OUT: (BNC Connector J9)	Modulated serial time code output.
7)	DC CODE: (BNC Connector J10)	Serial level shift time code output.
8)	SLOW CODE: BNC Connector J11)	Slow Code Output. Option A12A/A12B.
9)	EXT 1 MHz: (BNC Connector J12)	EXTernal 1 MHz time base input.
10)	UPDATE: (BNC Connector J13)	ID Number update input. P/O Option E13.
11)	WWV IN: (BNC Connector J14)	WWV In. Option S11A.
12)	EXT START: (BNC Connector J15)	Ext Start. Options S11/S11A.
13)	AC POWER: (AC Connector J101)	Mates with ac line cord.
14)	Interface: (36-pin connector J401)	Transport Control.
15)	STOP DELAY ADJ: (Potentiometer R3)	Set to the maximum time required for the transport to come to a stop from high speed.
16)	EXT/INT 1 MHz: (Slide Switch S32)	In the INTernal position, selects the internal 1 MHz oscillator. In the EXTernal position, selects the EXT 1 MHz through J12.
17)	365-366-ID: (Slide Switch S33)	Leap Year/ID select switch (P/O Days/ID Option E13).
18)	115/230 V Power Select: (Slide Switch S101)	Adapts power transformer for 115 or 230 V operation.

CHAPTER 4
MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

When the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns, when necessary. Address all inquiries on operation or applications to your nearest sales representative; or, Sales Manager:

SYSTRON-DONNER CORPORATION
CONCORD INSTRUMENT DIVISION
10 Systron Drive
Concord, California 94518
Phone: (415) 676-5000
TWX: 910-481-9479
Cable: SYSTRONDONNER

Specify both model and complete serial number in all correspondence.

4.2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1) Disconnect ac power and remove the top and bottom covers.
2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.
3) Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed-circuit board contains integrated-circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.
4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.
5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low-pressure stream of air to remove the foreign material.

CAUTION

Do not clean P.C. boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

6) Wipe the external surface of the instrument with a soft, damp cloth to remove dirt, fingerprints, and other foreign materials.

7) Replace the top and bottom covers and reconnect ac power. Perform the Operational Test and Calibration Procedure (Section 4.4). If performance does not match or exceed the specifications listed in Chapter 1 of this manual, corrective maintenance is in order.

4.3 PRINTED-CIRCUIT BOARD REPAIR

When replacing integrated circuits or other electronic components soldered to printed-circuit boards, the procedures indicated below must be followed or damage to the board may result:

1) Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2) Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component).

3) Apply heat (40-50 W soldering iron) sparingly to each of the cut pins or leads and remove from the board; clean the hole(s) with a toothpick or solder suction tool.

4) Form the tined leads of the replacement part and insert in the printed-circuit holes; solder, then trim leads to extend 1/16 inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16 inch diameter).

CAUTION

Always trim semiconductor leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.

5) When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the solder connection to cool before removing the heat sink.

6) Clean all dirt and solder-flux from the printed-circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

4.4 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the service engineer to isolate the trouble to a particular circuit card or subsection.

When the trouble is isolated, the functional description in Chapter 5 and option information in Chapter 6 will facilitate repair.

WARNING

Dangerous high voltages are present in the power supply of this equipment. Use caution at all times when the protective covers are removed.

4.4.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8154.

TABLE 4.1 TEST EQUIPMENT FOR MODEL 8154

Model	Manufacturer	Minimum Specifications
422	Tektronix, Inc.	Oscilloscope, 15 MHz bandwidth, triggered sweeps from 0.1 microseconds/cm to 5 sec/cm. Vertical sensitivity from .05 volts/cm to 20 volts/cm.
6012	Tektronix, Inc.	Probe, 10:1 attenuation ratio, 17 pF capacitance.
7004A	Systron-Donner Corp	DMM 10 MΩ input impedance ±0.1% accuracy.
200AB	Hewlett Packard	Audio Oscillator, 20 Hz to 40 kHz coverage.
6250	Systron-Donner	Frequency Counter, 0 Hz to 50 MHz, 3 parts/10^7 per week.

In addition to the equipment listed above, a suitable source of time code input signals with known characteristics is required. This may be a Time Code Generator or a prerecorded tape and tape playback equipment.

4.4.2 Power Supply Calibration Procedure (Dwg. #041810-7-9)

Check that fuse F1 is the proper size for the input voltage selected:

2A, 115 V

1A, 230 V

With an input of 115 V ac (230 V if so equipped) ±5%, 50/60 Hz. Check the following at the Power Supply P.C. Board, edge connector, P103.

1) +210 V ±25% at pins V, 18 (GND 20, X)
2) +21 V ±20% at pins S, 15 (GND BLACK TEST POINT)
3) +9 V ±20% at pins Y, 21 (GND BLACK TEST POINT)
4) -9 V ±20% at pin 2 (GND BLACK TEST POINT)
5) -21 V ±20% at pin 4 (GND BLACK TEST POINT)

Measure the +15 V supply on the BLUE (GND BLACK) Test Point and adjust R5 (15 V ADJ) for +15 V ±0.3 V.

Measure the -15 V supply on the VIOLET Test Point and verify that it is within ±0.3 V of -15 V. Readjust R5 is necessary so that both +15 and -15 V supplies are within ±0.3 V.

Measure the +5 V supply on the RED Test Point and adjust R19 (5 V ADJ) for 5 V ±0.1 V.

Measure the -5 V supply on the GREEN Test Point and verify that it is within ±0.1 V of -5 V. Readjust R19 is necessary so that both +5 and -5 V supplies are within ±0.1 V.

4.4.3 Oscillator

The accuracy of the oscillator may be determined, relative to a frequency standard, by observing the rate of an oscilloscope pattern as shown in Figure 4.1, Oscillator Accuracy Test.

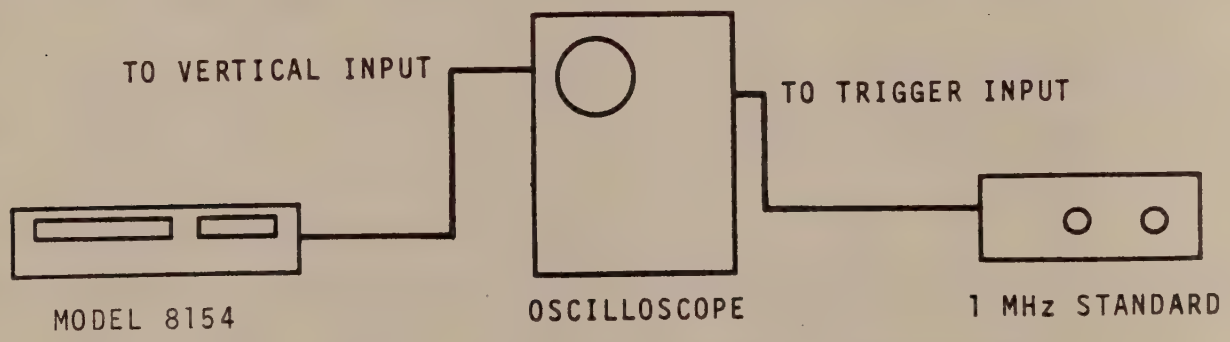


FIGURE 4.1 OSCILLATOR ACCURACY TEST

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard; if the pattern moves to the left, the frequency under test is too high.

To check oscillator frequency (not stability):

1) Trigger the oscilloscope externally with the 1 MHz standard.
2) Connect a 1 MHz frequency from the Model 8154 to the vertical input of the oscilloscope, (pin X of the Time Base Card).

3) Set the oscilloscope sweep time to 0.1 μsec/cm and adjust the controls to obtain a presentation of one to two cm vertical deflection.

4) Horizontal drift of the oscilloscope display in cm/sec is the difference from the standard frequency in parts/10^7. If necessary, adjust the oscillator (C3, on the Time Base Card) until drift is negligible.

TABLE 4.2 OSCILLATOR ACCURACY

Drift	Accuracy
1 cm/0.1 sec	1 part in 10^6
1 cm/sec	1 part in 10^7
1 cm/10 sec	1 part in 10^8

4.4.4 Generate Function

1) Place the MODE selection switch in the GENerate position to ensure that the DISPLAY COUNTER indexes in a normal sequence.

2) Preset 23 hours, 59 minutes, 59 seconds into the DISPLAY COUNTER and note that on the next count the display becomes all 0's (if the instrument also displays days, that the days register advances to 001).

3) Repeat Step 2) and preset 009 in the Days Register and observe that on the next count the days register will advance to 010.

4) Repeat Step 3) to ensure correct operation for the remaining digits of the days register.

4.4.5 Shaper & Modulator (Dwg. #021556-7-5)

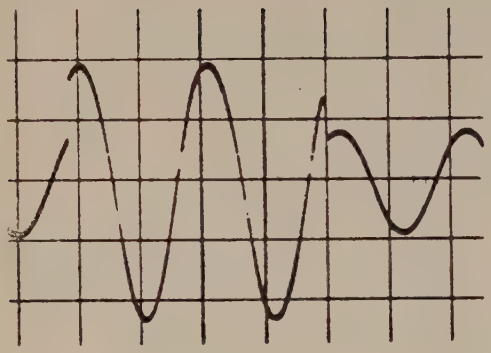
1) Adjust the TUNE control (R53) for maximum ac signal at the MOD test point.

2) Adjust the MOD CODE LEVEL control (R20) for a nominal 3 V p-p, output of the Large Cycle signal.

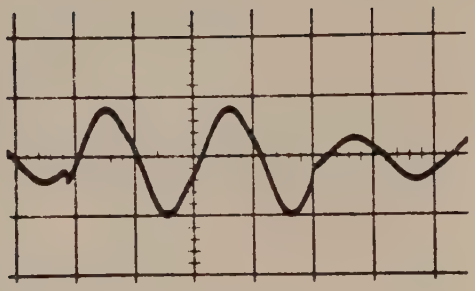
3) Adjust the RATIO control (R16) for a 3:1 modulation ratio.

4) Return to the TUNE control (R53) and adjust until the junction point of the large and small cycles has a minimum of distrotion, (see Figure 4.2, Tune Control Adjustment).

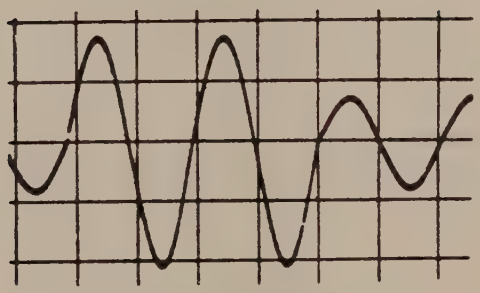
5) Adjust the DC CODE LEVEL control (R23) for a nominal output of 3 V p-p.



Incorrect
Adjust Tune Control CW



Incorrect
Adjust Tune Control CCW



Correct

FIGURE 4.2 TUNE CONTROL ADJUSTMENT

4.4.6 AGC & Cycle Detector Adjustment (Dwg. #021569-7-1)

Preliminary Set-Up

1) Connect Time Code Source to "Code In" BNC on rear panel of the unit. Adjust the input to approximately 3 V p-p.

2) Place unit in READ MODE.

CAUTION

Do not place AGC & Cycle Detector on extender board when performing these adjustments.

AGC Level Adjustment

Monitor "TRIG" Test Point with oscilloscope.

1) Adjust the AGC LEVEL ADJ (R4) control so that the large cycles (see Figure 4.3, AGC Level Adjustment) are 2.75 V p-p ±5%.

2) Reduce level of incoming code to approximately 1 V p-p.

3) Allow approximately 5 seconds for AGC to recover. Signal at "TRIG" Test Point should remain the same amplitude as adjusted in Step 1).

Cycle Detector Adjustment

Monitor "TRIG" Test Point with oscilloscope.

1) EC (Each Cycle) Adjustment.

   Set oscilloscope to trigger positive (+), external trigger.

   Connect external trigger input of oscilloscope to "EC" Test Point.

   Turn E.C. ADJ (R25) control full clockwise. Turn in the CCW direction until each cycle is triggering approximately 30% up on th the positive slope of the small cycles (see Figure 4.4, Cycle Detector Adjustment).

2) $\overline{\text{LLC}}$ (Lower Large Cycles) Adjustment:

   Set oscilloscope to trigger negative (-), external trigger. Connect external trigger input of oscilloscope to $\overline{\text{LLC}}$ Test Point.

   Turn L.L.C. ADJ (R34) control full clockwise. Turn in the CCW direction until the lower large cycles are triggering approximately 75% of the way down on the negative slope of the lower large cycles (see Figure 4.5, Lower Large Cycle Adjustment).

4.4.7 Reverse Operation

With the Model 8154 in the READ MODE, check that it will read in both the forward and reverse directions. (Press, momentarily, the FWD pushbutton for a forward code and the REV pushbutton for a reverse code).

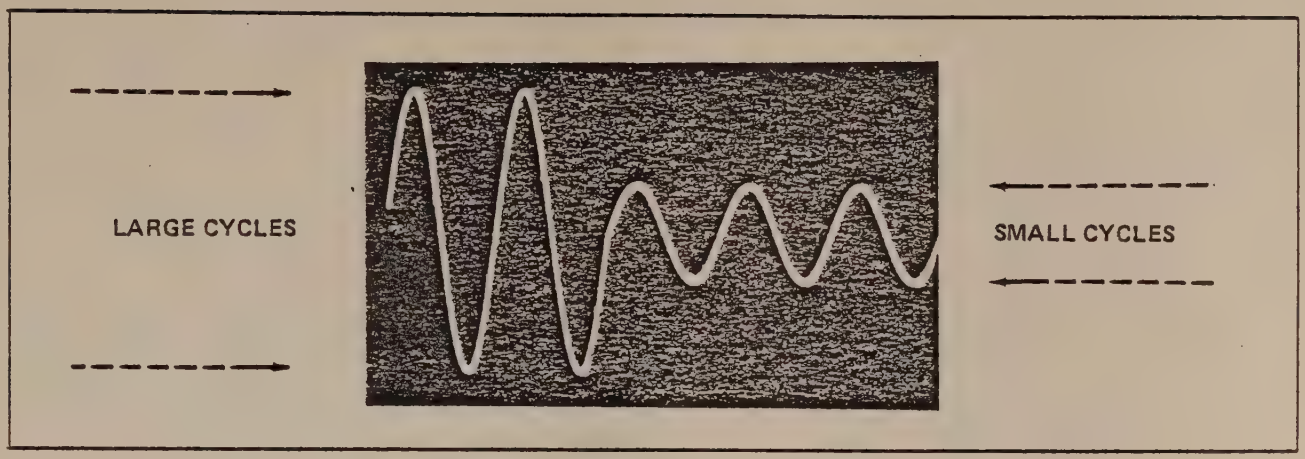


FIGURE 4-1 AGC LEVEL ADJUSTMENT

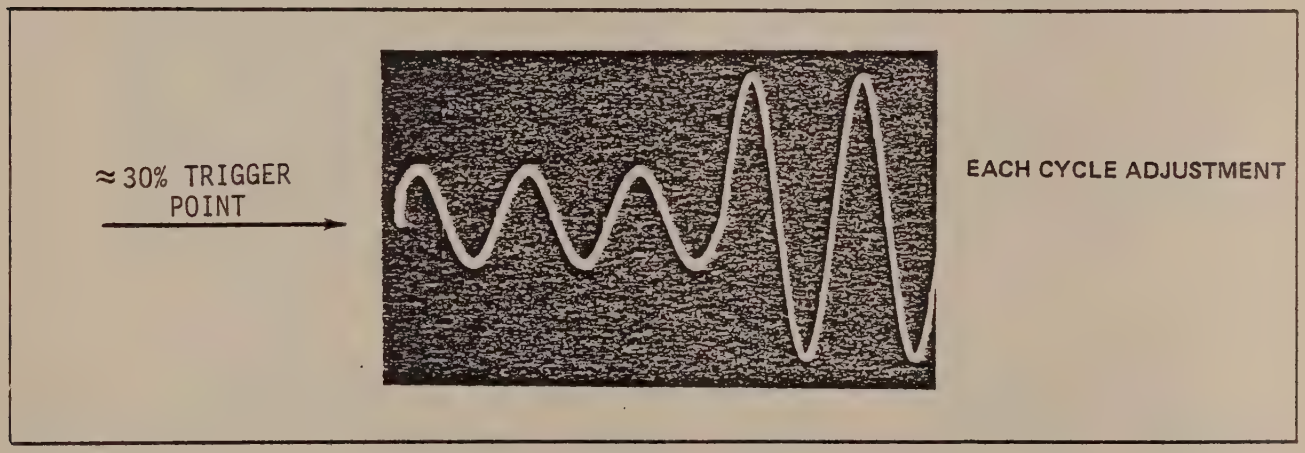


FIGURE 4-2 CYCLE DETECTOR ADJUSTMENT

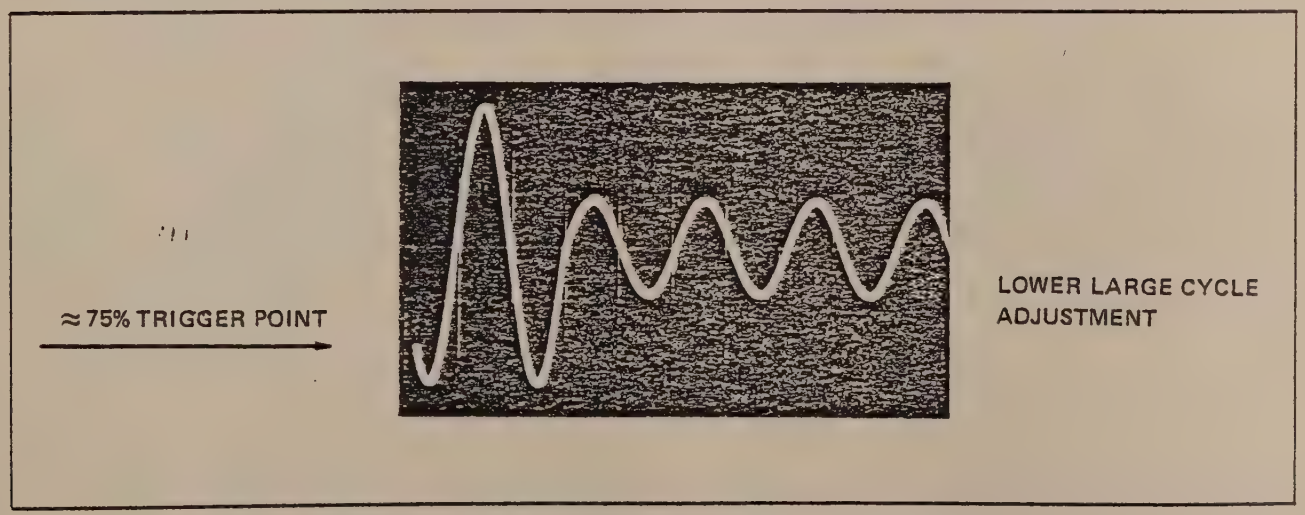


FIGURE 4-3 LOWER LARGE CYCLE ADJUSTMENT

4.4.8 Sensitivity

If possible, vary the input code voltage within the limits specified in Chapter 1 and observe that the unit reads the code in both forward and reverse.

4.4.9 Frequency Response

If possible, vary the rate of the input code within the limits of carrier frequency specified in Chapter 1 and observe that the unit reads normally in forward and reverse.

4.4.10 Error Bypass (Dwg. #7-05153802)

1) Using a separate time code generator with a HOLD mode; place the generator in HOLD and produce a continuous time code which is not updated. Connect this signal to the CODE IN BNC on the rear panel of the Model 8154.
2) Place the Model 8154 MODE selection switch in READ and the ERROR BYPASS in the ON position. Observe that the units-of-seconds updates 3 numbers and returns to the number displayed on the test generator.
3) Place the MODE switch in GENerate. The translator should update in the normal manner.

4.4.11 Stop Delay (Dwg. #05192905, Sheet 2)

Actuate the Stop Delay circuit by alternately pressing two different function control pushbuttons on the front panel. The STOP pushbutton is lighted during the Stop Delay time. Set the STOP DELAY ADJ control (R3) on the rear panel for a delay time longer than the longest time necessary for the transport to come to a complete stop. Range is approximately 1 to 15 seconds.

4.4.13 General Checkout

No additional adjustments are required in the instrument. To facilitate tracing possible malfunctions, determine if each plug-in card is performing in accordance with the circuit description provided in other sections of this manual. It is advisable to determine proper operation of the boards in the order of decreasing signal repetition rate. Peripheral circuits, such as thumbwheel switches, are most easily tested in conjunction with their associated plug-in boards.

CHAPTER 5

FUNCTIONAL DESCRIPTION

5.1 GENERAL

The Model 8154 is a combination Time Code Generator/Reader/Tape Search unit. These three main functions are described separately in this chapter. Schematics and specific card assembly descriptions relating to the basic unit are provided at the end of this chapter. Standard options, when included, are described in Chapter 6. Special modifications, if any, are presented in Chapter 7.

5.1.1 Reference Designations

Reference designations are confined to the assembly under discussion since it is usually clear from the context which assembly is involved.

When citing a subelement of a multielement integrated circuit, the reference designation of the integrated circuit is given, followed by the number of the output terminal.

When citing flip-flops formed from two gates on the same chip, the reference designation of the chip is given followed by the two output pin numbers. The reference designations used in the Model 8154 are listed in Table 5.1.

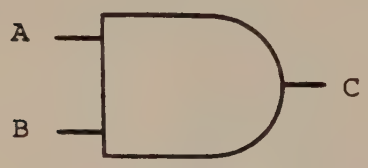
TABLE 5.1 REFERENCE DESIGNATIONS

A or U	Integrated Circuit
C	Capacitor
CR	Diode
DS	Lamp
F	Fuse
FL or Z	Filter
J	Jack
L	Inductor
P	Plug
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
W	Jumper
X	Socket

5.1.2 Logic Functions

The Logic symbols and functions used in the Model 8154 are described as follows:

AND Gate

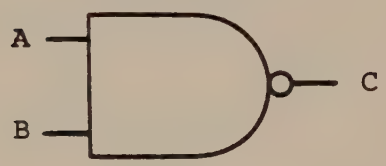


INVERTED NOR Gate

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

The AND Gate and INVERTED NOR Gate have the same truth table.

NAND Gate

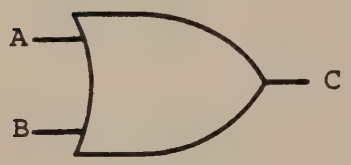


INVERTED OR Gate

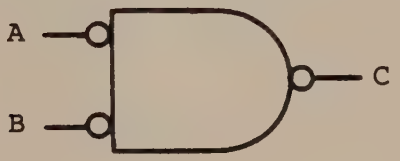
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

The NAND Gate and INVERTED OR Gate have the same truth table.

OR Gate



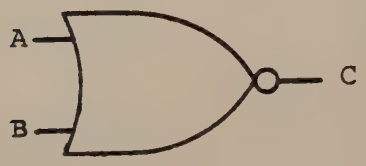
INVERTED NAND Gate



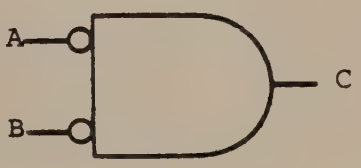
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

The OR Gate and INVERTED NAND Gate have the same truth table.

NOR Gate



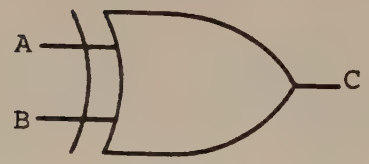
INVERTED AND Gate



A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

The NOR Gate and INVERTED AND Gate have the same truth table.

EXCLUSIVE OR

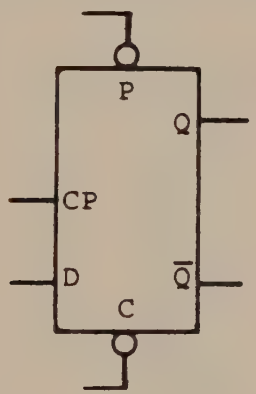


A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE NOR

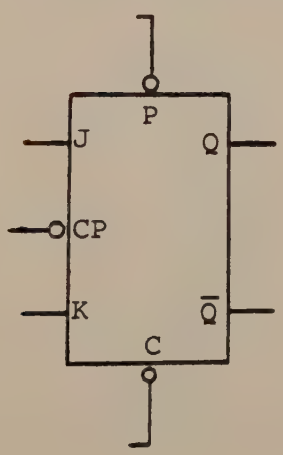
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

D-TYPE Flip-Flop



1) Q assumes the state of the D input on the positive transition of the clock (CP) input.
2) The D input is locked out when the clock input is positive.
3) P and C override all other inputs.
4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.
5) At a set condition, Q is Logic 1. At a clear condition, Q is a Logic 0.

JK-TYPE Flip-Flop



1) When J and K are both at a Logic 0, no change will occur.
2) When K is a Logic 1, Q will be a Logic 0.
3) When J is a Logic 1, Q will be a Logic 1.
4) When J and K are both at a Logic 1, the flip-flop will change state.
5) $\overline{P}$ and $\overline{C}$ override all other inputs.
6) $\overline{CP}$ is the clock input.

In some configurations it is possible to perform the AND and OR functions simply by tying the outputs of certain gates together.

These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line the AND or OR symbol is used only once.

DOT AND

DOT OR

5.1.3 Logic Nomenclature

The Logic nomenclature used to describe operation of the Model 8154 is given in Table 5.2.

TABLE 5.2 LOGIC NOMENCLATURE

A	Automatic Mode
A_B	Automatic Search to Start (Begin) Mode
AC	Axis Crossing
AGC	Automatic Gain Control
A_{RC}	Automatic Re Cycle Mode
A_{SC}	Automatic Single Cycle Mode
B	Start (Beginning) Time
BCD	Binary Coded Decimal
BLANK	BLANKing Signal for Function Relays
D	Drive (Playback)
DIS	DISconnect
E	Stop (Ending) Time
EC	Each Cycle
ES	Early Start
ERROR	ERROR Signal
F	Search or Fast Forward
FWD	ForWarD
HOLD	HOLD Mode
I	Interval
LLC	Lower Large Cycle
M	Manual Mode
MOMEN	MOMENtary Signal for Function Relays
N	Number of Frames of Overshoot
P	Pulse (Pushbutton Command)
P_D	Drive Pulse
P_F	Search or Fast Forward Pulse
P_R	Search or Fast Reverse Pulse
P_S	Stop Pulse

TABLE 5.2 LOGIC NOMENCLATURE (Cont'd)

R	Search or Fast Reverse
READ	READ MODE
REM	REMote
REV	REVerse
S	Stop
Sb	Strobe
SD	Stop Delay
SS	Search Speed
St	Stored
T	Transport
TD	Transport Drive
TF	Transport Search or Fast Forward
TOD	Time-of-Day
TR	Transport Search or Fast Reverse
TS	Transport Stop
1P/MS	One pulse per millisecond
1P/S	One pulse per second
1P/F	One pulse fer frame

5.2 GENERATOR FUNCTION

When functioning as a Time Code Generator this unit is essentially a digital clock which generates a serial time code. A 1 MHz time base signal is divided down to 1 pps and fed to a TOD Accumulator (Display Register) with parallel outputs; BCD time in hours, minutes and seconds. The accumulated time is displayed and (as an option) may be provided as buffered, parallel, BCD outputs at a rear panel connector. This same time information is serialized and fed to rear panel BNC connectors in dc level shift form and as a modified IRIG B time code on a 1 kHz carrier. (Days/ID and/or other codes may be provided as options.) Switches are provided for entering Start time for real time operation or the unit may be operated in an elapsed time mode.

The Generator circuitry is described below and in more detailed circuit descriptions at the end of this chapter. The circuit is shown in block form on Sheet 1 of the Block Diagram (Dwg. #7-05192905).

5.2.1 Time Base & Control (Dwg. #021566-7-11)

Referring to the Block Diagram, the Time Base & Control Card (A27), is shown at the left. This card contains the internal 1 MHz oscillator with shaper, a Start/Stop flip-flop, an Elapsed Time Gate, a three-decade divider and separate TOD and Days/ID Preset/Reset circuits. The symmetrical 1 kpps output (5×10^{-4}) from the divider is fed through selection gates on Preset & Error Bypass Card A11, emerging as the Z-RATE signal which is fed to Minor Counter Card, A9, and Code Generator Card A17. The inverse of this signal is fed to the Modulator Card A8, where it is shaped to form the 1 kHz carrier for the serial time code.

Preset/Reset circuitry is used in conjunction with the Comparator Cards (A18 & A19) and circuits on the Preset & Error Bypass Card (A11) to reset or serially preset the accumulator to the time entered on the START (PRESET) thumbwheel switches.

5.2.2 Minor Counter (Dwg. #021632-7-2)

The Minor Counter Card A9, is a three-decade divider which divides the 1 kHz ($\overline{\text{Z-RATE}}$) input down to 1 pps to drive the TOD Accumulator Card A15, and provide a sync signal for Code Generator Card A17. Separate sets of buffers are provided for parallel BCD Millisecond Outputs for Options E14 (Milliseconds Search) and E14A (Millisecond outputs). Pulse Rates (1 kpps, 100 pps, 10 pps and 1 pps) are provided at connector J7.

5.2.3 TOD Accumulator (Dwg. #021543-7-3)

The TOD Accumulator Card A15, accepts the 1 pps (8×10^{-1}) output from the Minor Counter Card A9, and divides it into units and tens of seconds, minutes and hours. The decade and scale-of-six dividers which accomplish this can be parallel preset, as well as provide parallel BCD outputs. The parallel BCD outputs feed; 1) the Display Card A102; 2) the Code Generator Card A17; 3) the Tape Search Comparator Cards A18 and A19; and 4) Buffer Card A16 to provide TOD Outputs (Option D15). The 1 ppd output is fed through selection gates on the Modulator Card A8 to Days Accumulator Card A21 as part of Days/ID (Option E13).

5.2.4 Code Generator (Dwg. #021554-7-1)

The Code Generator Card A17, accepts the parallel TOD (and Day) inputs and develops a serial level shift code complete with index and frame markers. Days/ID are replaced by zeros in the code in the absence of Option E13. The level shift code is fed to the Modulator Card A8.

5.2.5 Modulator (Dwg. #021556-7-5)

The Modulator Card A8, modulates a synchronized 1 kHz sine wave with the serial level shift code from the Code Generator Card A17. The 1 kHz sine wave is developed by shaping the Z-RATE input previously mentioned. The modulated and level shift (dc) codes are buffered; then fed to rear panel BNC connectors. Adjustments for mark-to-space ratio and amplitude are provided.

5.3 READER FUNCTION

As a Time Code Reader, this unit accepts a serial modulated IRIG B time code input. It strips time information from the code in bytes, and loads it into the TOD Accumulator Card A15. The time in the accumulator is displayed. It is also available for output in parallel BCD as an option. Circuits are included to maintain the accumulator on time in forward, and to regenerate a serial code for comparison with the input in the ERROR BYPASS Mode of operation. (Days/ID and/or the translation of other time codes may be included as Options.) Most of the Reader circuitry is shared with the Generator described above, as shown on Sheet 1 of the Block Diagram (Dwg. #7-05192905).

5.3.1 AGC/Cycle Detector (Dwg. #021569-7-1)

Referring to the Block Diagram, the modulated input code is fed through J8 to the AGC/Cycle Detector Card A10. The AGC circuit on this card establishes a standard level signal from which two signals are derived. The first of these is the EC (Each Cycle) signal which is a square wave at the carrier frequency. The second is the LLC (Lower Large Cycle) signal. Both signals are fed to the Reader Logic Card A12. The EC signal is also fed through selection gates on Preset & Error Bypass card A11, emerging as the $\overline{\text{Z-RATE}}$ signal to the Minor Counter Card A9, and Code Generator Card A17.

5.3.2 Reader Logic (Dwg. #021588-7-3)

The Reader Logic Card A12, contains a 9-bit shift register which accumulates time information stripped from the input code. This register is cleared and a ONE entered by the double mark at the beginning of the time frame. This is followed by each subsequent bit as it is detected. When the initial ONE is in the 9-position, the contents of the shift register are transferred into the seconds section of the TOD Accumulator Card A15. The next index mark clears the register and enters a ONE followed by minutes information. These bits are transferred to the minutes section of the accumulator. In like manner, hours (and days) bits are detected and transferred. (Days are loaded into Days Accumulator A21.)

5.3.3 Minor Counter (Dwg. #021632-7-2)

Once the Reader is synchronized with the input code (in forward) the Accumulator, consisting of Card A15 (plus Card A21 with Option E13) already contains the current information being transferred in. This is made possible by the Minor Counter Card, A9, which derives a 1 pps, "on-time" update pulse from the $\overline{\text{Z-RATE}}$ signal. This signal updates the accumulator "on-time" at the beginning of each frame.

5.3.4 Error Bypass (Dwg. #7-05153802)

The Code Generator Card A17, accepts the parallel TOD (and Day) information and develops a serial level shift output code as previously described for Generator Function. This code, which represents the contents of the accumulator, is compared with the incoming code in circuits on the Preset & Error Bypass Card A11, when operating in the ERROR BYPASS Mode. This circuitry inhibits the transfer of up to three consecutive input code frames when a discrepancy is detected.

5.3.5 Modulator (Dwg. #021556-7-5)

The Modulator Card A8, supplies the regenerated dc level shift code as an output. When operating in real time, the regenerated modulated code is also available.

5.3.6 Reverse Code

When operating in READ or any of the SEARCH Modes, the Time Code Reader is capable of reading the input code in reverse. The conditions for reverse Read operation are established by circuits on FWD-REV Control Card A13, in response to signals from the Tape Search section and the FWD and REV pushbuttons. Circuits on Card A13 invert the order in which bits are transferred to the Accumulator, kill the 1 pps update signal, and inhibit Error Bypass when reading a reverse code. In reverse, the contents of the Accumulator are no longer on-time.

5.4 TAPE SEARCH FUNCTION

The Tape Search section of the Model 8154 combined with the Reader section and the tape transport under control form a Tape Search System. The Tape Search section consists of; 1) a full comparator with related logic to compare the Reader output with preselected Start and Stop times; 2) control logic to implement both automatic and manual search operations; and 3) the transport control interface. (Search Days/ID and Search Milliseconds may be added to the basic unit as options.) The Search section is shown on Sheet 2 of the Block Diagram (Dwg. #7-05192905).

5.4.1 Comparator Circuits (Dwg's #021501-7-1, #021513-7-1 & #021583-7-1)

Referring to the Block Diagram, the Comparator consists of TOD and Days Comparator Cards A18, A19 and A22, the TOD, Days and Milliseconds START and STOP thumbwheel switches S1 through S24, and the Comparator Logic formed from circuitry on Cards A23 (Comparator Logic) and A24 (Mode Logic). The optional Days and MS circuits are shown in dotted outline.

Parallel BCD Days and TOD input data from the tape unit under control is fed to the Comparator Cards from the Accumulator in the Reader. These data are compared with the parallel BCD Days and TOD data entered on the START or STOP thumbwheel switches, which are also connected to the Comparator Cards. Each Comparator Card contains circuitry for the full High/Low comparison of 12 bits (3-digits). The cards are connected in tandem and the final outputs are fed to the Comparator Logic circuits on Card A23. The "$\geq$" output assumes the "1" state if the input data from the Reader is greater than or equal to the switch-entered data. The "$\leq$" output assumes the "1" state if the converse is true. The most significant bits dominate. Both outputs are "1" when the two sets of data are equal. Referring to Schematic #021583-7-1 of Comparator Logic Card A23, the "$\geq$" and "$\leq$" signals are combined and fed to gates controlled by the Error Signal from the Error Bypass circuit on Card A11. If more than three frames are in error, comparisons are rejected. The outputs of the "error" gates represent the ">", "=" or "<" status of tape time relative to the switch-entered Start time. Only one set of these switches is armed at any given time.

The decision is made by Start/Stop flip-flop A9 located on Mode Logic Card A24. The complementary outputs, B and E, from this flip-flop are fed to Comparator Logic Card A23, where they control the Start and Stop switch enable circuitry (Q3 and Q4) and are combined with the ">", "=" and "<" signals. In addition, they generate Interval level (I) and Start and Stop Pulse outputs.

A one-pulse-per-second (tape time) signal ($\overline{1\ P/S}$) from the Reader (connected to Card A23) fires a 10 μs Strobe Delay one-shot on the trailing edge "on-time". The output of the Strobe Delay, in turn, fires the Strobe one-shot on the trailing edge. The resulting Strobe signal gates comparison signals to the Control Circuits. It is delayed to provide time for the Comparator to propagate and settle. These comparison signals are labeled Sb<B, $\overline{Sb<B}$, Sb>B, $\overline{Sb>B}$ and Sb>E. In addition a Sb=B signal is generated which sets the Start/Stop flip-flop A9 on the trailing edge, provided the unit is operating in one of the Automatic Modes and is in DRIVE.

When the Milliseconds Option (E14) is included, the Sb>E and Sb=B signals are strobed at a one-pulse-per-millisecond rate (by the 1 P/MS input). The 1 P/MS signal and parallel BCD MS data come from the Minor Counter Card A9 in the Reader. The MS data are fed directly to the MS Start (S10,S11,S12) and Stop (S22,S23,S24) switches. The switch commons are dot ANDED with the Sbm$\overline{s}$B and Sbm$\overline{s}$E lines on Comparator Logic Card A23, respectively. These lines are held clamped to ground at all times except when the associated control gate is enabled (B or E positive), the 1 P/MS Strobe is positive, and the incoming MS data are in coincidence with the time set on the respective MS START or STOP switches.

The <B and $<\overline{B}$ lines are not Strobed. These, along with "I", are fed to lamp drivers on Drivers Card A26. The associated lamps, which are labeled "<", ">", and "INT", indicate when tape time is less than or greater than Start time, and when the tape time is in the interval between the Start and Stop frames.

5.4.2 Control Circuits (Dwg's #021512-7-3, #021513-7-1 & #021583-7-1)

The Control circuitry consists of the following sub-blocks: 1) Function Logic; 2) Mode Logic; 3) Stop Delay; 4) Momentary; 5) Overshoot; and 6) Early Start.

The Control circuits establish the mode of operation and, on the basis of manually entered commands along with signals from the Comparator, generate control and status signals which are fed to the Reader and transport control interface.

The operating modes are selected by MODE Switch S30. The Modes are broken into two categories: Automatic and Manual. Automatic operation will be described first. The 3 standard Automatic Modes are: 1) Search to Start; 2) Single Cycle; and 3) Recycle (discussed in that order).

With the exception of the $\overline{DIS}$ line all MODE switch lines are wired to the Mode Logic circuit on Card A24. This is shown on Schematic Dwg. #021513-7-1. The $\overline{DIS}$ line is wired directly to a driver on Drivers Card A26 which energizes the Disconnect Relay (K DIS) in all SEARCH Modes. It is also fed to the Function Logic Card A25, where it disarms the FWD, REV and DRIVE pushbuttons, and imposes a STOP condition in the GEN/READ Modes of operation.

Refer to Mode Logic Schematic #021513-7-1. The Mode Logic circuit consists of inverters and inverted OR gates which establish the required logic level signals. These are labeled A, A_B, A_{RC}, M, $A_{RC}+A_{SC}$, and $A_{SC}+A_B$. The 4-input NAND gates form a 5-state flip-flop, in combination with gate A3-6, which is controlled by ground pulses on the MODE switch lines.

The mode logic level signals are fed to the Function Logic, on Card A25, along with the comparison signals from the Comparator Logic. Referring to Function Logic Schematic #021512-7-1, these signals are fed to the 4-state flip-flop and the related Start-Time-Store flip-flop.

The function pushbuttons FWD (P_F), REV (P_R), DRIVE (P_D) and STOP (P_S) are dot ANDED with the control gate lines to the 4-state flip-flop. This flip-flop has the characteristic that only one of the 4-outputs ($\overline{F}$,$\overline{R}$,$\overline{D}$, and $\overline{S}$) can exist in the ground state at any given time, with the particular output determined by which control line was pulled to ground last. In addition, when a particular control line is first grounded, the flip-flop immediately locks and ignores subsequent transitions and noise on that line. It is, therefore, immune to contact bounce. If two or more buttons are pressed simultaneously, all outputs go positive, producing a condition equivalent to disconnect; the final state is determined by the pushbutton released last.

Transistor Q1 ensures that the circuit is awakened in Stop by momentarily grounding the P_S (STOP) line when power is first applied. It also forces the instrument into Stop when the MODE switch is first turned to the MANUAL position.

The function pushbuttons may be used to override automatic operation at any time. (They are disabled in PRESET and GEN Modes.)

5.4.3 Search-to-Start

When in the (SEARCH) TO START Mode, the A, A_B and $A_{SC}+A_B$ lines from the the Mode Logic circuit are positive, establishing the conditions for Search-to-Start operation. Referring to Figure 5.1, the Auto Control Cycles for the Model 8154, the sequence of operation shown by path ABCDEF is described first. This is followed by a discussion of the alternate paths JD'KBCDEF, C'DEF and MB'C'DEF.

Starting from Stop, the ABCDEF sequence is initiated by pressing the FWD pushbutton. Referring to Function Logic Schematic #021512-7-3, the $\overline{S}$ output from the four-state flip-flop is at ground. When the FWD

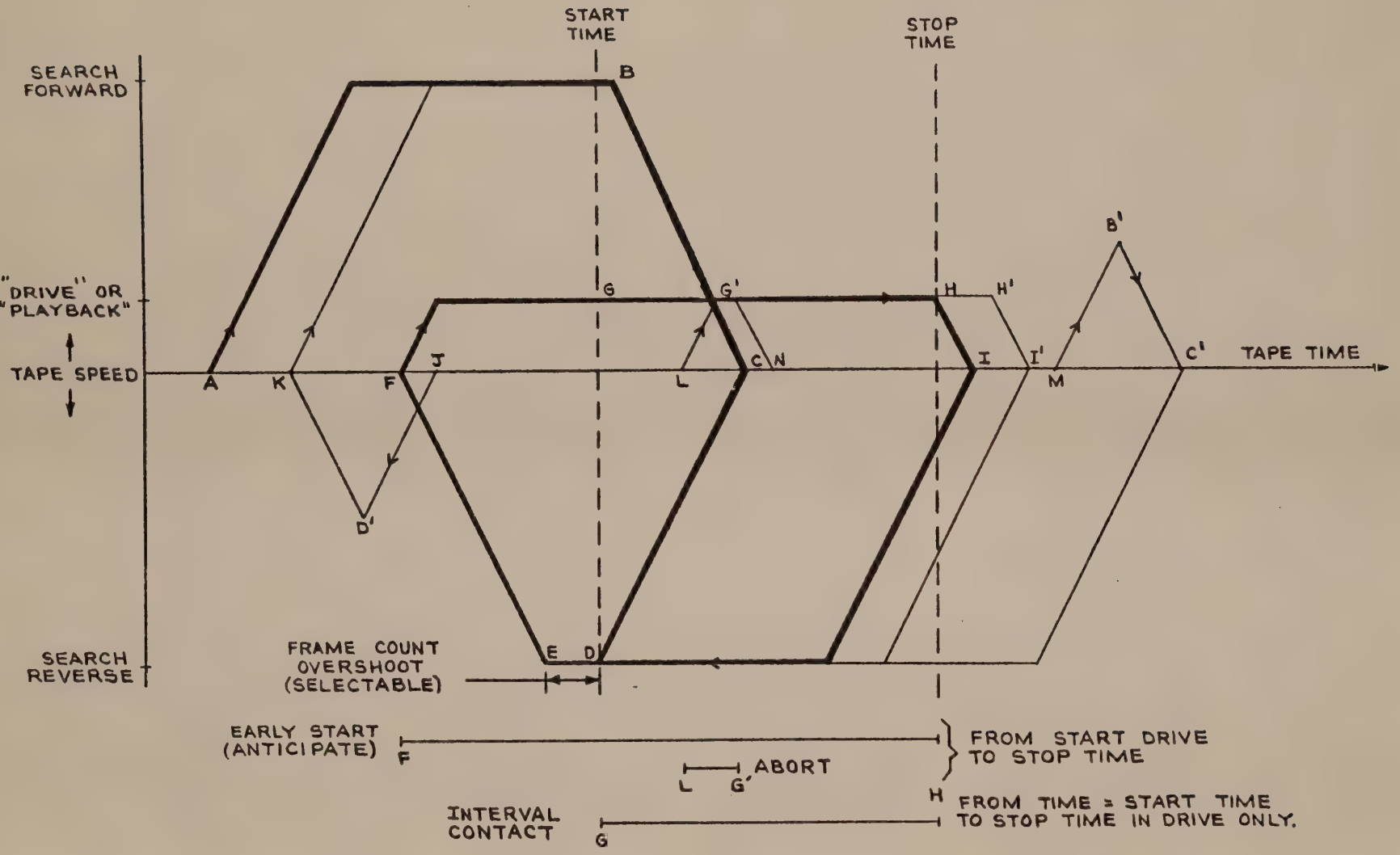


FIGURE 5.1 AUTO CONTROL CYCLES FOR MODEL 8154

pushbutton is pressed, control line P_F is grounded, forcing $\overline{S}$ positive and the $\overline{F}$ output to ground. The $\overline{F}$ output is inverted and fed to a lamp driver on Drivers Card A26; this turns on the lamp mounted in the FWD button. In addition, it is gated and fed as line TF to a relay driver also on A26. A description of the Stop Delay and Momentary circuits on Mode Logic Card A24 is now necessary before continuing with the discussion of the Search-to-Start function.

Refer to Schematic #021513-7-1. When triggered, the Stop Delay circuit output ($\overline{SD}$) goes to ground for a period of time which is adjustable over a range of approximately 1 to 15 seconds. The purpose of this Stop Delay signal is to temporarily place the transport in the Stop condition when changing from one functional mode to another; thus, it is permitted to come to a full stop before commanding the new mode. There is no need, however, to delay entering a new mode if the transport is already in Stop. In this case, the Stop Delay is defeated by the $\overline{S}$ input which inhibits operation. Under all other conditions, the circuit is triggered whenever one of the control inputs P_F, P_R or P_D goes to ground.

The Momentary circuit has two inputs, $\overline{SD}$ and $\overline{S}$. These are fed to an inverted OR gate (A8) which initiates a 14 ms Blanking signal ($\overline{BLANK}$) and a longer (140 ms) Momentary (MOMEN) signal whenever the gate output changes state. This output, labeled TS, is also fed to a relay driver on Drivers Card A26. Referring to Drivers Schematic #021515-7-1, this circuit is one of a group of six transport relay drivers (Q1 through Q6) which (with the exception of Q6) are fed the $\overline{BLANK}$ output from the Momentary circuit. The MOMEN output is also fed to the Momentary Bus through driver circuit Q7,Q8 for operation of the transport control relays.

Returning to the aforementioned functional description, when the FWD pushbutton is pressed, the P_F line goes to ground before the $\overline{S}$ line goes positive; the Stop Delay circuit is not triggered. The $\overline{SD}$ output from Function Logic Card A25 remains positive and its complement, DS is at ground. With the positive transition of $\overline{S}$, both inputs ($\overline{S}$ and $\overline{SD}$) to the Momentary circuit are positive and the output, TS, goes to ground; thus, the input to the Stop relay driver is removed triggering the generation of $\overline{BLANK}$ and MOMEN pulses at the output.

The first five transport relay drivers on Drivers Card A26 are turned off during the $\overline{BLANK}$ signal time. This ensures that any previously energized relay has a chance to drop out before the next relay picks up, and prevents any contact bridging when the transport relays are wired for latched operation. The Q6 driver is not used in this unit.

The TF line, from the Function Logic Card A25, controls the first transport relay driver. The output grounds the coil of KF relay at the end of the blanking time, energizing it. The relay may be wired to stay energized until the next mode is commanded (latched operation), or may be allowed to drop out at the end of the momentary time.

The transport is commanded into Fast Forward (Search Forward) by the KF relay and follows path A to B on Figure 5.1. The time code read from the tape during this time is less than the time entered on the Start switches. If this were not the case, path MB'C'DEF would be followed instead of ABCDEF. When the Comparator detects the first frame greater than Start time, the Sb>B line sets the Start-Time-Store flip-flop on Function Logic Card A25. This flip-flop was previously reset by the S signal prior to starting the sequence. In addition, the Sb>B line goes positive. It is fed to a control gate (A1) on Card A25. The other two inputs to this gate (A & F) are also positive at this time. Output P_R, therefore, goes to ground setting the 4-state flip-flop in the R state and triggering the Stop Delay circuit. The R output is inverted and fed to a lamp driver on Drivers Card A26 which turns on the lamp in the REV pushbutton. The lamp in the FWD pushbutton is turned off. The SD signal from the Function Logic triggers the Momentary circuit on Mode Logic Card A24. The TS output from the Momentary circuit turns on the Stop relay-driver, which turns on the lamp in the STOP pushbutton.

At the end of the Stop Delay time, the transport is at a standstill at point C on Figure 5.1. The TR signal goes positive and the TS line returns to ground, turning off the STOP lamp and triggering the Momentary circuit. The Reverse relay is energized and the transport moves in Fast Reverse (Search Reverse) to point D.

It is now necessary to look at the Overshoot circuit on Comparator Logic Card A23, Schematic #021583-7-1. The scale-of-16 binary counter is in reset (clear); the counter had been placed in this condition by the $\overline{R}$ line of the Function Logic when it was at ground. It counts $\overline{1\ P/F}$ signals gated by the <B signal. The symbol N represents a number of frames and is fixed at three in this unit. The N<B signal goes positive after three frames less than Start time have been counted. The purpose of this overshoot is to ensure that after the transport has come to a stop at point F on the "Auto Control Cycles for Model 8154" diagram, there are a sufficient number of frames for the Reader/Search system to get into synchronism with the tape time code after being placed in DRIVE, and before reaching the Start time frame.

The N<B signal is fed to a control gate on Function Logic Card A25, along with three other signals (A_B, R and St>B), which are all positive at this time. When the N<B signal goes positive at point E, the output P_S, goes to ground. The 4-state flip-flop is forced into the $\overline{S}$ state The REV pushbutton lamp is turned off, the STOP pushbutton lamp is turned on, the Stop relay is operated, the Overshoot counter and Start-Time-Store flip-flop are reset. The transport is now in Stop at point F. It can be placed in Drive by pressing the DRIVE pushbutton. Operation in Drive is described later.

The sequence described by path ABCDEF is now completed. This path was followed because when the FWD pushbutton was pressed at the beginning of the sequence, the transport happened to be at a point on the tape which was less than the preset Start time. Pressing the REV pushbutton instead, causes the path to be JD'KBCDEF; this sequence description follows.

When the REV pushbutton is pressed, the transport is commanded into Fast Reverse following a series of events analogous to those which followed the operation of the FWD pushbutton. In this case, however, a different control gate on Function Logic Card A25 is open since inputs A, R and St>B are all positive. When the first Sb<B signal is received from the Comparator, the output P_F is pulled to ground; the transport is commanded into Fast Forward after an intervening Stop Delay. From this point on, operation and the path followed are identical to those described above for the basic ABCDEF sequence.

If the point on tape had been greater than Start time when the REV pushbutton was pressed, the transport would have been commanded into Fast Reverse. The first Sb>B signal from the Comparator would have set the Start-Time-Store flip-flop, and reset the Overshoot counter. The path followed (C'DEF) involves the same events as the CDEF portion of the basic path.

If, when the FWD pushbutton was pressed, the point had been greater than Start time, the transport would have been commanded into Fast Forward. However, the control gate output P_R would have gone to ground commanding the transport into Fast Reverse (with an intervening Stop Delay) when the first Sb>B signal was generated, and the path followed would have been MB'C'DEF.

5.4.4 Single Cycle

In the SINGLE CYCLE Mode, the Mode Logic Card A24, outputs A, $A_{SC}+A_B$, and $A_{RC}+A_{SC}$ are positive. Operation is identical to Search-to-Start Mode to point E on the "Auto Control Cycles for Model 8154."

It will be recalled that in Search-to-Start mode, a Stop control gate on Function Logic Card A25 was open and commanded the transport into Stop when the N<B signal went positive at point E. In SINGLE CYCLE Mode, this gate is closed since the A_B line is at ground. The Drive control gate is open instead, and commands Drive and Stop Delay. The D signal is inverted and ANDed with the next $\overline{Sb<B}$ signal. The output after being inverted, resets the Start-Time-Store flip-flop. The Overshoot counter is reset by the signal returning to ground as before. The transport enters Drive at point F after the Stop Delay period has elapsed. Subsequent operation is along path FGHI. This same path is followed when the DRIVE pushbutton is pressed after reaching point F in the SEARCH TO START Mode. The following discussion applies equally to both situations.

The TD output from Function Logic Card A25 goes positive at point F. The STOP pushbutton lamp is turned off, the DRIVE Pushbutton lamp is turned on, and the Drive relay energized. When the Start time frame is reached, a Sb=B signal eminates from the Comparator Logic Card A23 and sets the Start/Stop flip-flop. The B and E otuputs change state, arming the STOP switches. The transport continues in Drive until the Stop-time frame is detected at point H. At this time, a Sb≥E signal is generated and fed to a Stop control gate on Function Logic Card A25

which is open since inputs $A_{SC}+A_B$ and D are both positive. The resulting P_S ground signal sets the 4-state flip-flop to the $\overline{S}$ state, commanding the transport into Stop at point I. The Start/Stop flip-flop is reset by the D line returning to ground and the START switches are rearmed.

If the Start frame is not detected (no Sb=B output), the Start/Stop flip-flop will not be set and the first Sb>B signal from the comparator will command the transport to Stop (abort) along path G'N. This is accomplished by a Stop control gate on A25. If the Stop frame is not detected (no Sb=E output), then the first Sb>E signal will terminate the sequence along path H'I'. If the DRIVE pushbutton is pressed after the transport has come to a Stop beyond the Start time, the transport will be commanded into Drive and the first Sb>B signal will command it back into Stop along path LG'N.

5.4.5 Recycle

The RECYCLE Mode is identical to Singel Cycle up to point H or H'. At this time, Fast Reverse and Stop Delay are initiated by a Reverse control gate on Function Logic Card A25 and the transport returns to point D along path HID, or alternate path H'I'D; the cycle is repeated until the STOP pushbutton is pressed. All three of the Stop control gates on Card A25 are inhibited in the RECYCLE Mode.

5.4.6 Manual

In the MANUAL Mode, the automatic (A) logic lines from the Mode Logic Card A24 are all at ground, disabling the Automatic Control circuitry, the Overshoot circuit, and all aspects of comparator operation, with the exception of the "<" and ">" Start-Time lamps. These provide a visual indication of the relationship between tape time and the time entered on the Start time switches. The Stop time switches are disabled and may be ignored.

All functional (pushbutton) controls are operational, as are the Stop Delay and Momentary circuits. Referring to Function Logic Schematic #021512-7-3, all control gates to the 4-state flip-flop are disabled and the switch inputs (P_F, P_R, P_D and P_S) are the only active inputs. The flip-flop is automatically placed in the $\overline{S}$ (Stop) by Q1 when the MODE switch is first turned to the MANUAL position. It can be changed to different states only by pressing one of the pushbuttons. It will continue in a particular state until commanded to change by the manual operation of a pushbutton.

5.4.7 Transport Control Interface (Dwg's #021515-7-1 & #7-061400)

The Transport Control Interface consists of relay drivers on Drivers Card A26. Relay Assembly A401, and the Interface cables to the transport. (Interface Cable information is presented in the Appendix.)

Refer to the Relay circuitry on Schematic #7-061400. Relays K4, K6, K7, K8 and K9 control the operation of the transport. As mentioned previously, these relays can be wired for momentary or latched operation. The latching circuit is the switched +21 V Bus which is energized in all Modes except DISCONNECT. The Momentary Bus is driven from a circuit on Drivers Card A26 which is controlled by the MOMEN signal, or whenever the STOP pushbutton is pressed. As shown on Sheet 2 of Dwg. #7-05192905, a second set of contacts on STOP switch S29, connects SW+21 V to the Momentary Bus, thus, providing an alternate direct control path to the Stop relay, K4.

The Search Speed Relay K7, is energized in the Forward and Reverse high speed SEARCH Modes. It is used to select the Search Speed on transports in which the tape is lifted off the heads during fast operation or in which the tape cannot be read at the uncontrolled fast speeds.

The transport control relay contacts are wired to J401 where they are connected as required to the particular transport under control.

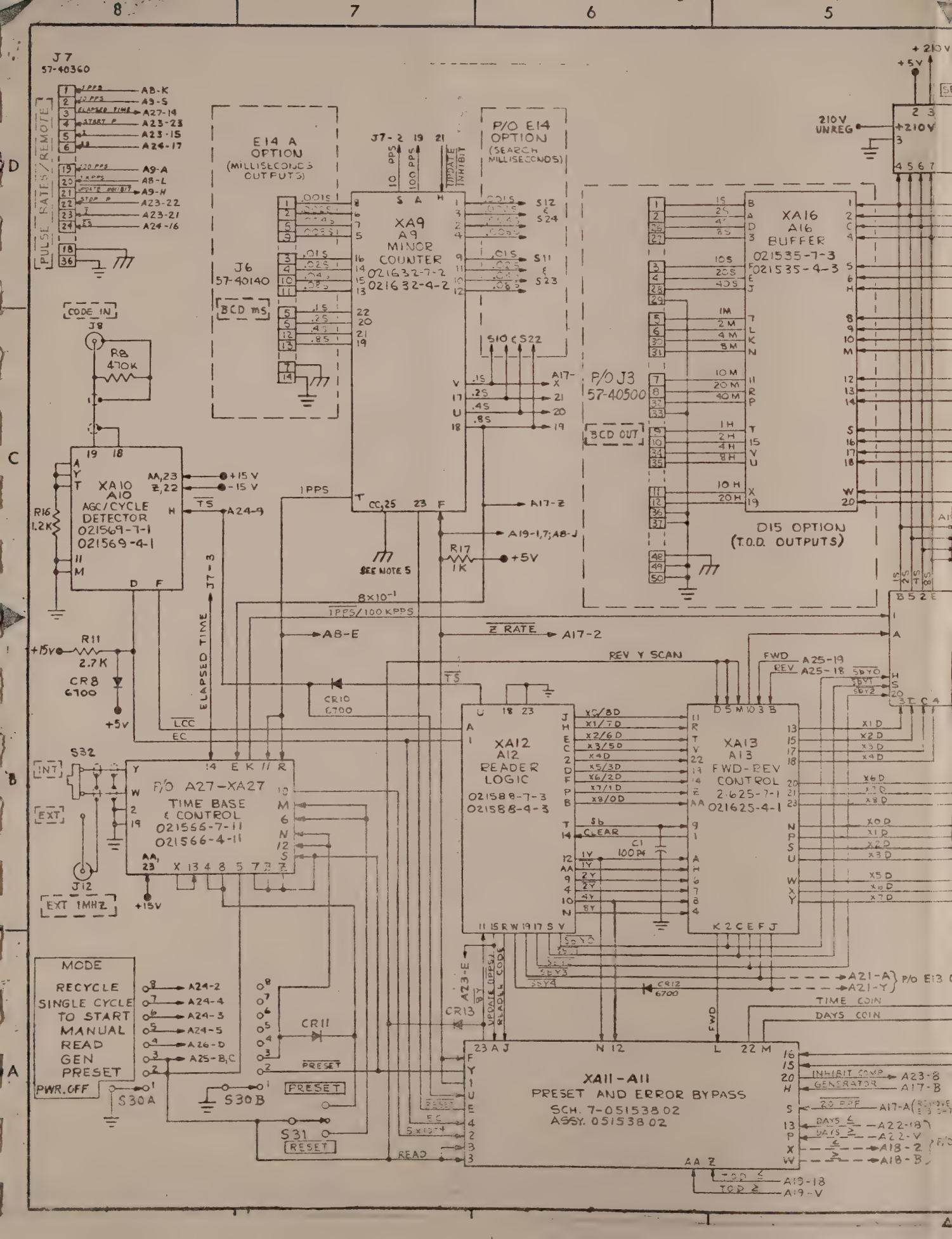
TABLE 5.3 CIRCUIT DESCRIPTION INDEX INFORMATION

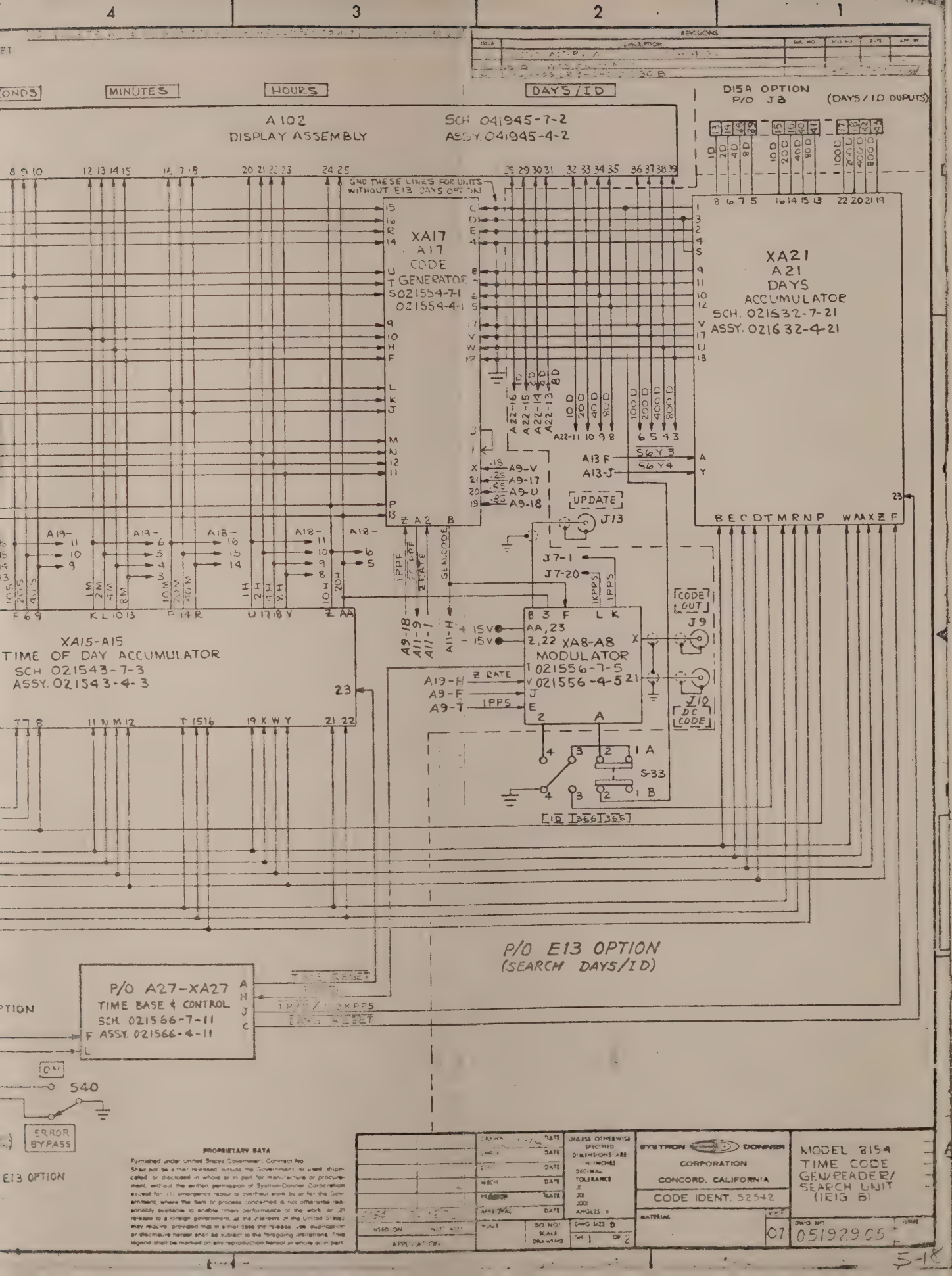
Location	Description	Schematic #	Page #
A1-A7	Reserved for Options		
A8	Modulator	021556-7-5	5-53
A9	Minor Counter	021632-7-2	5-82
A10	AGC/Cycle Detector	021569-7-1	5-64
A11	Preset & Error Bypass	7-05153802	5-87
A12	Reader Logic	021588-7-3	5-73
A13	FWD/REV Control	021625-7-1	5-77
A14			
A15	TOD Accumulator	021543-7-3	5-41
A16	Buffer (Optional)	021535-7-3	
A17	Code Generator	021554-7-1	5-48
A18	Comparator	021501-7-1	5-25
A19	Comparator	021501-7-1	5-25
A20			
A21	Days Accumulator (Optional)	021632-7-5	
A22	Comparator (Optional)	021501-7-1	
A23	Comparator Logic	021583-7-1	5-69
A24	Mode Logic	021513-7-1	5-33
A25	Function Logic	021512-7-3	5-29
A26	Drivers	021515-7-1	5-37
A27	Time Base & Control	021566-7-11	5-59
A101	Power Supply	041810-7-9	5-92
A102	Display Assembly	041945-7-2	5-99
A401	Relay Assembly	041810-7-9	5-92

All plug-in modules are designed so that the card will only fit into position if it is correctly aligned; however, caution must be exercised to ensure that a card is installed in the correct card slot. Extractor handles on all cards are numbered to facilitate correct installation.

CAUTION

When mounting a card on the extender board it is possible to install the card backwards which will result in serious damage.


J7
57-40360
PULSE RATES/REMOTE
E14 A OPTION
(MILLISECONDS OUTPUTS)
J6
57-40140
BCD MS
XA9
A9
MINOR COUNTER
021632-7-2
021632-4-2
P/O E14 OPTION
(SEARCH MILLISECONDS)
S10 & S22
S12 & S24
S11 & S23
CODE IN
J8
R8
470K
XA10
A10
AGC/CYCLE DETECTOR
021569-7-1
021569-4-1
R16
1.2K
R11
2.7K
CR8
6700
+15V
-15V
+5V
TS
A24-9
1PPS
ELAPSED TIME
JT-3
SEE NOTE 5
R17
1K
A17-Z
A19-1,7;A8-J
8x10⁻¹
1PPS/100 KPPS
AB-E
Z RATE
A17-2
REV Y SCAN
FWD
REV
A25-19
A25-18
P/O J3
57-40500
BCD OUT
XA16
A16
BUFFER
021535-7-3
021535-4-3
D15 OPTION
(T.O.D. OUTPUTS)
XA12
A12
READER LOGIC
021588-7-3
021588-4-3
XA13
A13
FWD-REV CONTROL
2-625-7-1
021625-4-1
CLEAR
C1
100 PF
CR10
6700
CR12
6700
CR13
S32
INT
EXT
J12
EXT 1MHZ
P/O A27-XA27
TIME BASE & CONTROL
021555-7-11
021566-4-11
LCC
EC
MODE
RECYCLE
SINGLE CYCLE TO START
MANUAL READ GEN PRESET
PWR.OFF
S30A
S30B
S31
PRESET
CR11
READ
XA11-A11
PRESET AND ERROR BYPASS
SCH. 7-051538 02
ASSY. 051538 02
TIME COIN
DAYS COIN
INHIBIT COMP GENERATOR
A23-8
A17-B
A17-A
A22-18
A22-V
A18-2
A18-B
A19-18
A19-V
P/O E13
+210V
210V UNREG



4
3
2
1
REVISIONS
MINUTES
HOURS
DAYS/ID
A102
DISPLAY ASSEMBLY
SCH 041945-7-2
ASSY. 041945-4-2
D15A OPTION
P/O J3
(DAYS/ID OUPUTS)
GND THESE LINES FOR UNITS WITHOUT E13 DAYS OPTION
XA17
A17
CODE
GENERATOR
S021554-7-1
021554-4-1
XA21
A21
DAYS
ACCUMULATOR
SCH. 021632-7-21
ASSY. 021632-4-21
UPDATE
J13
CODE OUT
J9
DC CODE
J10
XA15-A15
TIME OF DAY ACCUMULATOR
SCH 021543-7-3
ASSY. 021543-4-3
XA8-A8
MODULATOR
021556-7-5
021556-4-5
S-33
P/O E13 OPTION
(SEARCH DAYS/ID)
P/O A27-XA27
TIME BASE & CONTROL
SCH. 021566-7-11
ASSY. 021566-4-11
S40
ERROR BYPASS
E13 OPTION
PROPRIETARY DATA
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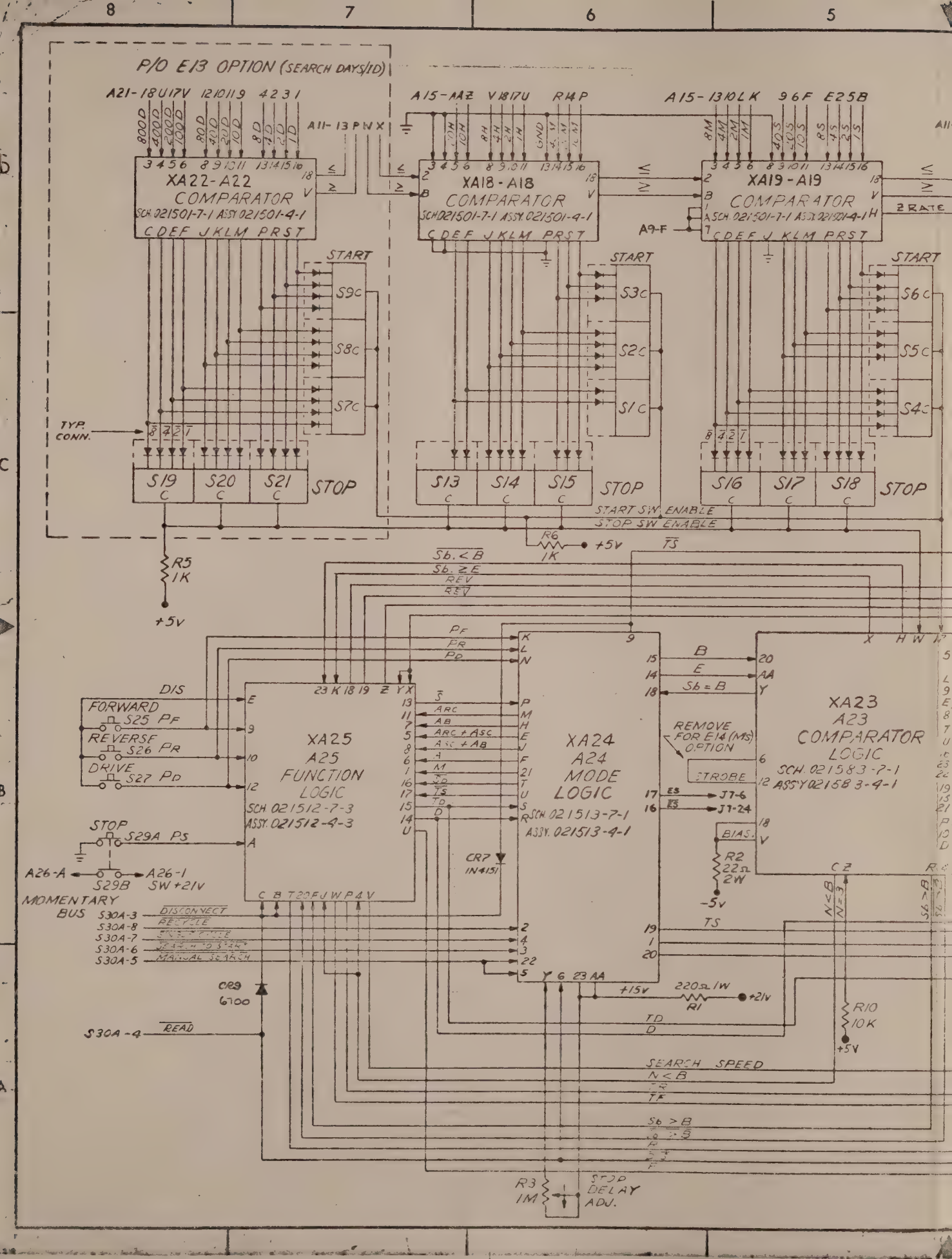
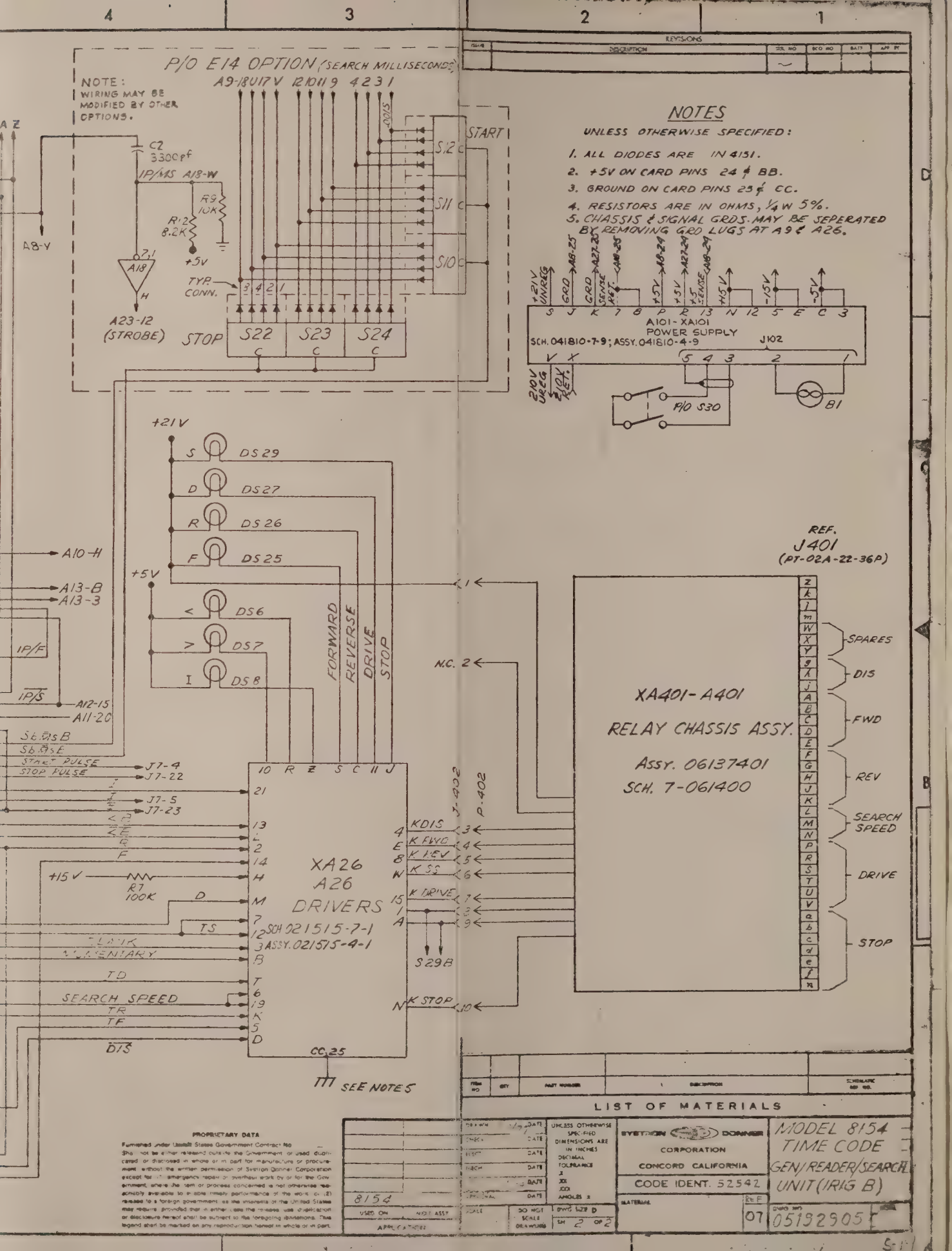
MODEL 8154
TIME CODE
GEN/READER/
SEARCH UNIT
(IRIG B)
07
051929C5
5-18


P/O E13 OPTION (SEARCH DAYS/ID)
XA22-A22
COMPARATOR
SCH 021501-7-1 ASSY 021501-4-1
XA18-A18
COMPARATOR
SCH 021501-7-1 ASSY 021501-4-1
XA19-A19
COMPARATOR
SCH. 021501-7-1 ASSY 021501-4-1
START
STOP
S9C
S8C
S7C
S3C
S2C
S1C
S6C
S5C
S4C
S19
S20
S21
S13
S14
S15
S16
S17
S18
TYP. CONN.
START SW ENABLE
STOP SW ENABLE
R6 1K
+5V
R5 1K
XA25
A25
FUNCTION
LOGIC
SCH 021512-7-3
ASSY. 021512-4-3
XA24
A24
MODE
LOGIC
SCH 021513-7-1
ASSY. 021513-4-1
XA23
A23
COMPARATOR
LOGIC
SCH. 021583-7-1
ASSY 021583-4-1
REMOVE FOR E14 (MS) OPTION
STROBE
BIAS
R2 22Ω 2W
-5V
DIS
FORWARD S25 PF
REVERSE S26 PR
DRIVE S27 PD
STOP S29A PS
S29B
A26-A
A26-1
SW +21V
MOMENTARY BUS
S30A-3 DISCONNECT
S30A-8 RECYCLE
S30A-7 SEARCH TO START
S30A-6 SEARCH TO END
S30A-5 MANUAL SEARCH
S30A-4 READ
CR9 6100
CR7 IN4151
+15V
220Ω 1W
R1
+21V
R10 10K
TD
TS
SEARCH SPEED
N<B
S6>B
R3 1M
STOP DELAY ADJ.



P/O E14 OPTION (SEARCH MILLISECONDS)
NOTE: WIRING MAY BE MODIFIED BY OTHER OPTIONS.
A9-18 U17 V 12 10 11 9 4 2 3 1
START
S12
S11
S10
C2 3300pf
IP/MS A18-W
R9 10K
R12 8.2K
+5V
A18
A23-12 (STROBE)
TYP. CONN.
STOP
S22
S23
S24
A8-Y
NOTES
UNLESS OTHERWISE SPECIFIED:
1. ALL DIODES ARE IN 4151.
2. +5V ON CARD PINS 24 & BB.
3. GROUND ON CARD PINS 25 & CC.
4. RESISTORS ARE IN OHMS, 1/4 W 5%.
5. CHASSIS & SIGNAL GRDS. MAY BE SEPERATED BY REMOVING GRD LUGS AT A9 & A26.
+21V UNREG
GRD
GRD
SENSE RET.
+5V
+5V
+5 SENSE
+15V
-15V
-5V
A101-XA101
POWER SUPPLY
SCH. 041810-7-9; ASSY. 041810-4-9
J102
210V UREG
210V RET.
P/O S30
B1
+21V
DS29
DS27
DS26
DS25
+5V
DS6
DS7
DS8
FORWARD
REVERSE
DRIVE
STOP
A10-H
A13-B
A13-3
IP/F
IP/S
A12-15
A11-20
START PULSE
STOP PULSE
J7-4
J7-22
J7-5
J7-23
+15V
R7 100K
TS
TD
SEARCH SPEED
TR
TF
DIS
XA26
A26
DRIVERS
SCH 021515-7-1
ASSY. 021515-4-1
CC.25
SEE NOTE 5
KDIS
K FWD
K REV
K SS
K DRIVE
K STOP
S29B
J-402
P-402
N.C. 2
REF.
J401
(PT-02A-22-36P)
XA401-A401
RELAY CHASSIS ASSY.
ASSY. 06137401
SCH. 7-061400
SPARES
DIS
FWD
REV
SEARCH SPEED
DRIVE
STOP
REVISIONS
LIST OF MATERIALS
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8154
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CONCORD CALIFORNIA
CODE IDENT. 52542
MODEL 8154
TIME CODE
GEN/READER/SEARCH UNIT (IRIG B)
07
05192905

PARTS LIST

FINAL ASSEMBLY #7-05192905

REF.	DESCRIPTION	SD PART NO.
	SHIPPING ASSEMBLY REV A	05192905
	Assembly, Test	05193004
	Trim, Front	04199711
	Trim, Strip Insert	04177411
	Trim, Side	03985905
	Trim, Rack Mount End	03995202
	Window	05100111
	Cover, Mounting Bracket	039857
	Cover, Top	3376005
	Cover, Bottom	03376105
P7	Connector, 36-pin Mating (Amph 57-30360)	101158
P101	Cord, Line	102407
P401	Connector, PTO GA-22-365	101213
	Handle	100927
	Support, Rear	03995102
	TEST ASSEMBLY REV B	05193004
	Schematic	7-05192905
A8	Modulator	021556-4-5
A9	Minor Counter	021632-4-2
A10	AGC/Cycle Detector	021569-4-1
A11	Preset and Error Bypass	05153802
A12	Reader Logic	021588-4-3
A13	FWD/REV Control	021625-4-1
A15	Time-of-Day Accumulator	021543-4-3
A17	Code Generator	021554-4-1
A18,19	Comparator	021501-4-1
A23	Comparator Logic	021583-4-1
A24	Mode Logic	021513-4-1
A25	Function Logic	021512-4-3
A26	Drivers	021515-4-1
A27	Time Base and Control	021566-4-11
A29	Extender	021507-4-1
	Assembly, Rear Panel	05193101
	Assembly, Front Panel	05193101
	Assembly, Power Supply	05194101
	Relay	041810-4-9
		06137401

REF.	DESCRIPTION	SD PART NO.
C1	Capacitor, MICA, 100 pf	100173
CR7	Diode, 1N4151	100385
CR8-10,12	Diode, 6700	006700
J402	Connector, Rectangular, 12 pos. Molex	102809
R1	Resistor, 220 Ω 5%, 1 W, CC	102037
R2	Resistor, 22 Ω 5%, 2 W, CC	101655
R5,6,17	Resistor, 1 k 5%, ¼ W, CC	101569
R7	Resistor, 100 k 5%, ¼ W, CC	101558
R8	Resistor, 470 k 5%, ¼ W, CC	101630
R10	Resistor, 10 k 5%, ¼ W, CC	101570
R11	Resistor, 2.7 k 5%, ¼ W, CC	101599
R16	Resistor, 1.2 k 5%, ¼ W, CC	101581
P102	Connector, Shell, 5 pos. Molex	101263
	Connector, Terminal, Male	10282202
XA1,8-13,15, 17-19,23-27	Connector, P.C. Board	101204
	Connector, P.C. Edge, 44 contacts	101167
XA101	Connector, Modification	051066-4-1
	Connector, Key	102653
	Pin Terminal, 1561 Molex	10282201
	Standoff	100494
	Gusset, Left	041809-1-1
	Gusset, Right	041809-1-2
	Card Guide	021340-1-2
	Card Rack, Front	08115501
	Card Rack, Rear	08115502
	Spacer Plate, Power Supply	051121-1-1
	Relay Shield	061373
	REAR PANEL ASSEMBLY REV F_1	05193101
	Panel, Rear	051931
B1	Fan	1008038
J3,5	Cover Plate, 50 pin	031394-1-1
J6	Cover Plate, 14 pin	021398-1-1
J7	Connector, 36 pin	101176
J8-10,12	Connector, BNC	101155
(P102-1,-2)	Connector Contact	10282202
R3	Resistor, 1 M 20%, ½ W, Var.	102878
S32	Switch, Slide, DPDT	102630
S33	Cover Plate, Slide Switch	05120802
	Cover Plate, BNC	100952

PARTS LIST

FINAL ASSEMBLY #7-05192905 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
	Insulator, BNC	100823
	Fan Screen	100886
	#6 Flat Washer	100704
	#6 Hex Nut	100706
	#6 Shake	100647
	Ground Lug, BNC	100495
	Screw, 2-56 x ¼L, PHMS	10062504
	Nut, 2-56	100636
	Washer, Int. Tooth, #2	100701
	FRONT PANEL ASSEMBLY REV F_4	05194101
	Panel, Front Sub	051935
	Assembly, Display, 6 digit	041945-4-2
DS6-8	Lamp	101130
DS6,8	Lens, White	10089901
DS7	Lens, Amber	10089902
DS25-27,29	Lamp	101140
XDS6-8	Lamp Holder	100899
S1,3,5,13, 15,17	Switch, Thumbwheel, with colon	05130002
S2,4,6,14, 16,18	Switch, Thumbwheel	05130001
S25-27,29	Actuator Push Button Mom.	102342
S25	Display Screen Engraving	02171211
S26	Display Screen Engraving	02171212
S27	Display Screen Engraving	02171213
S29	Display Screen Engraving	02171215
(S29)	Contact Block (2 each)	10234201
S30	Switch, Rotary, 2 pole, 8 pos. w/ac	06134433
S31	Switch, Toggle, DPDT, Mom.	102333
S40	Switch, Toggle, 4 PDT	102310
	Trim Strip	04177311
	Spacer, .35 wide	102358
	Mtg. Strap, 9 digit	10236709
	Bracket, End Mounting	102359
	Dress Nut	100893
	Knob	102954
	Screw, 4-40 x ¼, FHMS	101031

CIRCUIT DESCRIPTION
COMPARATOR
SCHEMATIC #021501-7-1

1) GENERAL

The Comparator card compares two parallel, 3 BCD-digit (12 bits) inputs and produces two outputs. Two or more cards may be connected in tandem to accommodate 6, 9, or more BCD digits (24, 36 or more bits). The inputs may also be straight binary.

One set of parallel inputs is connected to the numbered input pins 3-6, 8-11, and 13-16, and the other set is tied to lettered input pins C-F, J-M, and P-T. They are connected in sequence with the most significant bits at pins 3 and C. When connected in tandem, the output pins 18 and V of the more significant card are connected to input pins 2 and B, respectively, of the less significant card.

Output pin 18 assumes the "1" state if the set of parallel inputs to the numbered side is less than, or equal to the set of parallel inputs to the lettered side. Output pin V assumes the "1" state if the set of numbered inputs is larger than or equal to the set of lettered inputs. This characteristic applies to each bit stage in the comparator with the most significant bits dominating the final outcome.

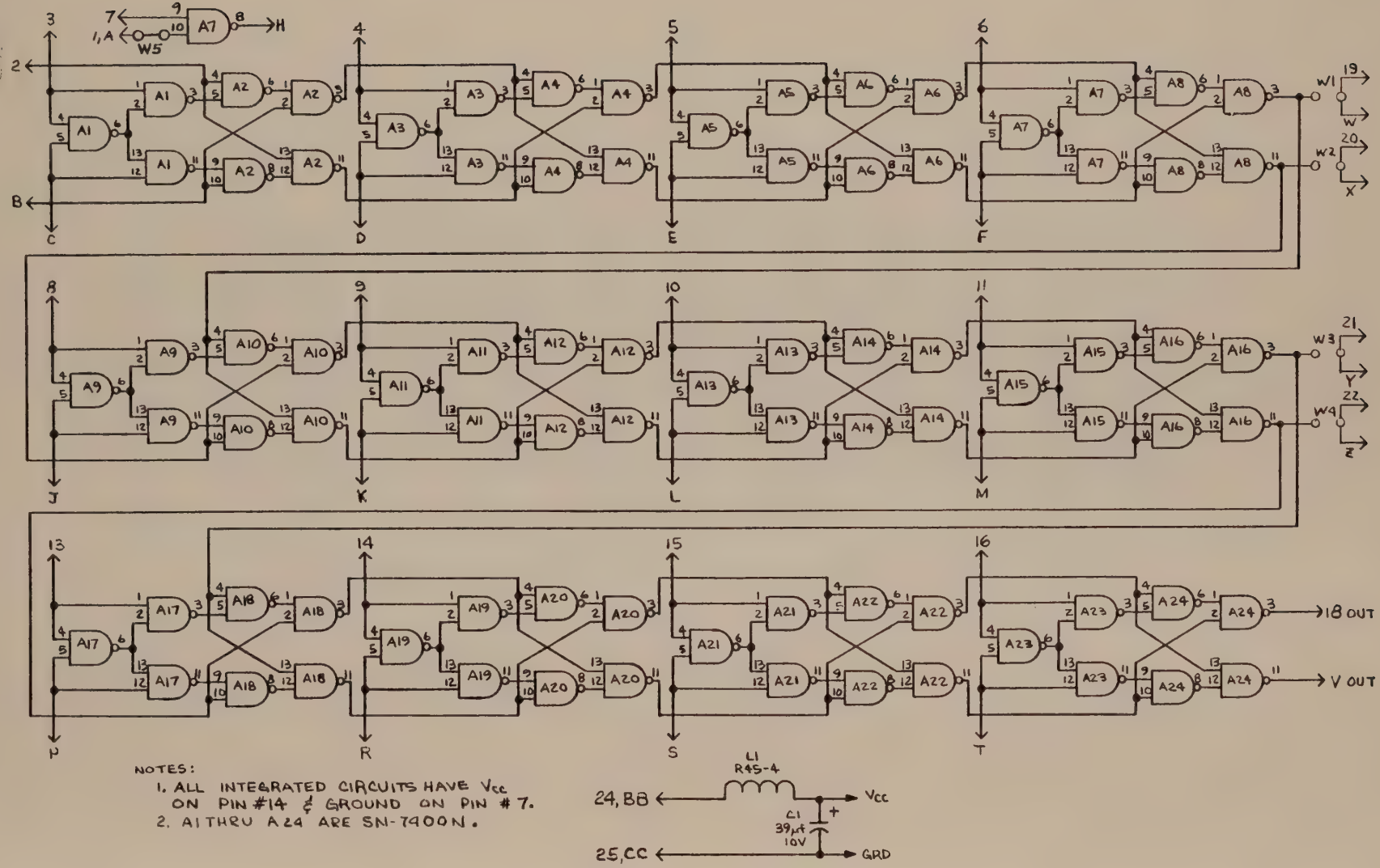
If inputs 2 and B are left open ("1" state) or are driven to the "1" state by the outputs from a more significant card, this implies that the more significant bits (if any) are equal and the final decision as to the relative magnitudes of the two sets of inputs is left to the first bit stage, in the remainder of the chain, which detects a difference.

Referring to the first bit stage on the card, where bits connected to pins 3 and C are compared, gate outputs A1-3 and 11 are in the "1" state if the two input bits are both "0" or both "1". Then, if the inputs to pins 2 and B are both "1" as we have stipulated, the gate outputs A2-3 and 11 will also both be "1" and the decision passes to the next lower stage.

If input pin 3 is "1" and input pin C is "0", however, gate A1-3 will be "0" and A1-11 will be "1". This drives A2-3 to the "0" state while A2-11 remains at the "1" state. These outputs are fed to the next stage where A2-3 drives A4-6 and A4-11 to the "1" state, and A2-11 combined with A4-6, drives A4-3 to the "0" state. The A4-3 and 11 outputs will assume these states, regardless of the status of the inputs to pins 4 and D. These established states at A4-3 and 11 will propagate through the remaining stages of the comparator, forcing pin 18 to "0" and pin V to "1", and ignoring all bits of lower significance.

If input pin 3 is "0" and input pin C is "1" the opposite condition is established and propagated through the comparator to the outputs.

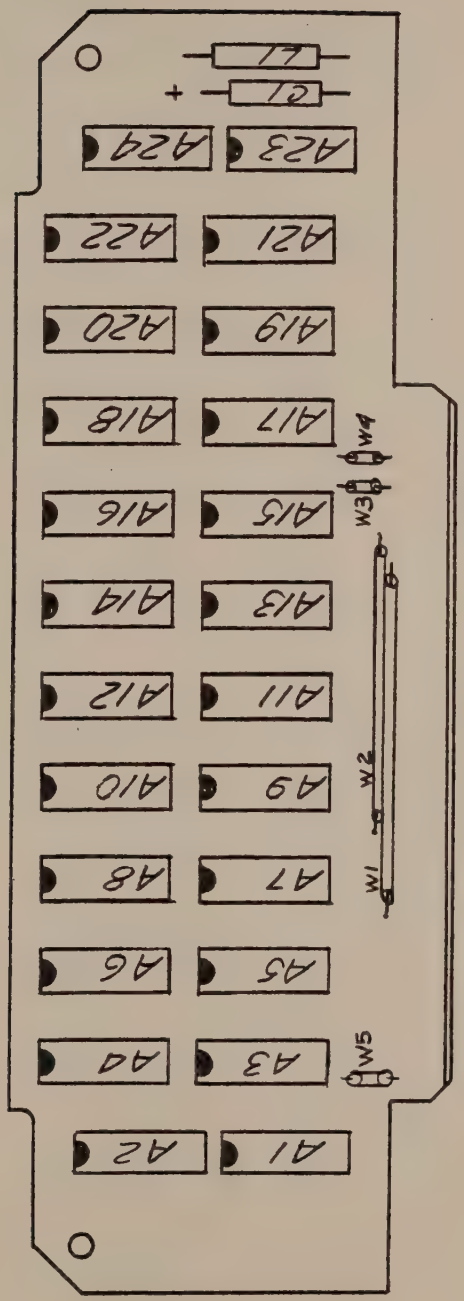
For equality (both outputs "1") the bits of one set of parallel inputs must be identical to the equivalent bits of the other set throughout the sequence.



NOTES:

1. ALL INTEGRATED CIRCUITS HAVE Vcc ON PIN #14 & GROUND ON PIN # 7.
2. A1 THRU A24 ARE SN-7400N.

COMPARATOR SCHEMATIC #021501-7-1 (REV E)



COMPARATOR ASSEMBLY #021501-4-1D

PARTS LIST

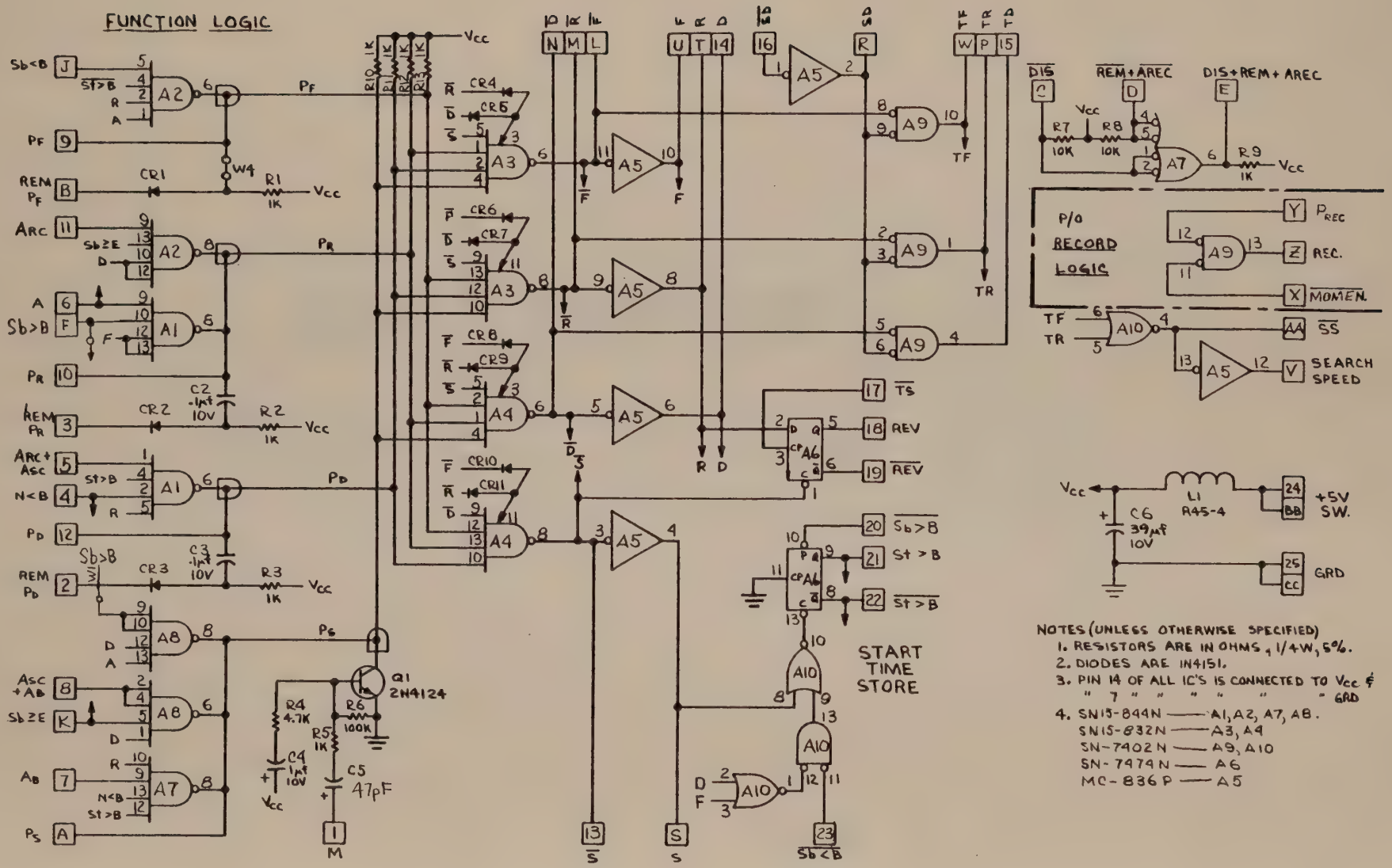
COMPARATOR #021501-7-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021501-4-1
	Schematic	021501-7-1
A1-24	Integrated Circuit, SN7400N	019705
C1	Capacitor, 39 µF, 10 V	100183
L1	Inductor, R45-4	101313
W5	Wire, 24 Ga., Insulated	
	Extractor	100865

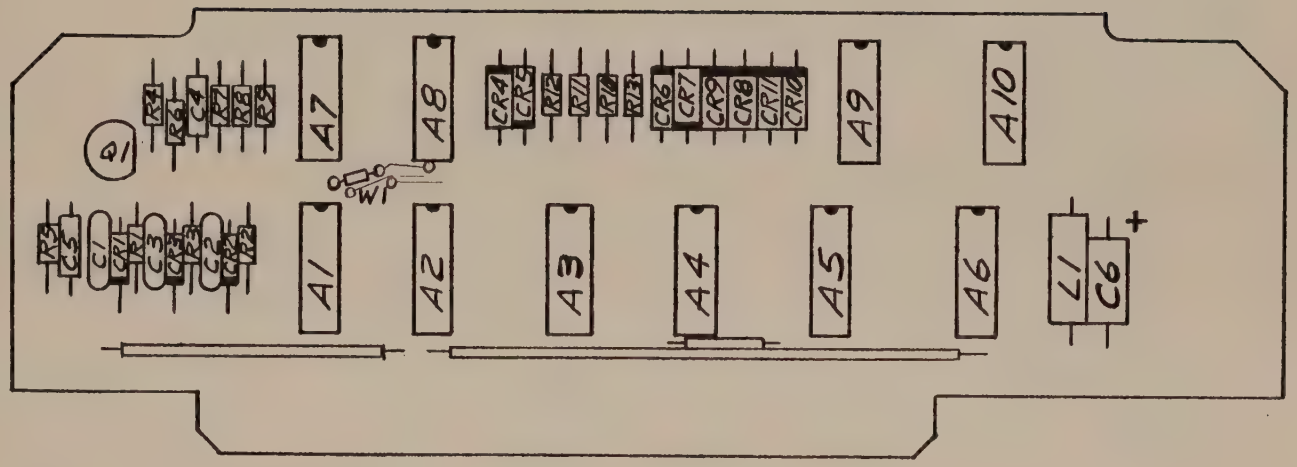
CIRCUIT DESCRIPTION
FUNCTION LOGIC
SCHEMATIC #021512-7-3

1) GENERAL

The Function Logic card is one of a group of three cards which contain the comparator and control logic circuitry. The other two are the Comparator Logic card A23 and the Mode Logic card A24. The functional descriptions of the circuitry on these two cards are provided in Sections 5.4.1 and 5.4.2.



FUNCTION LOGIC SCHEMATIC #021512-7-3



REF NOTES

W1 TIES A8,9,10 TO PIN F
W2 " " " " " H
W3 REPLACES CR1
W4 " C1
W5 " CR2
W6 " C2
W7 " CR3
W8 " C3

FUNCTION LOGIC ASSEMBLY #021512-4-1 REV B,

PARTS LIST

FUNCTION LOGIC #021512-7-3

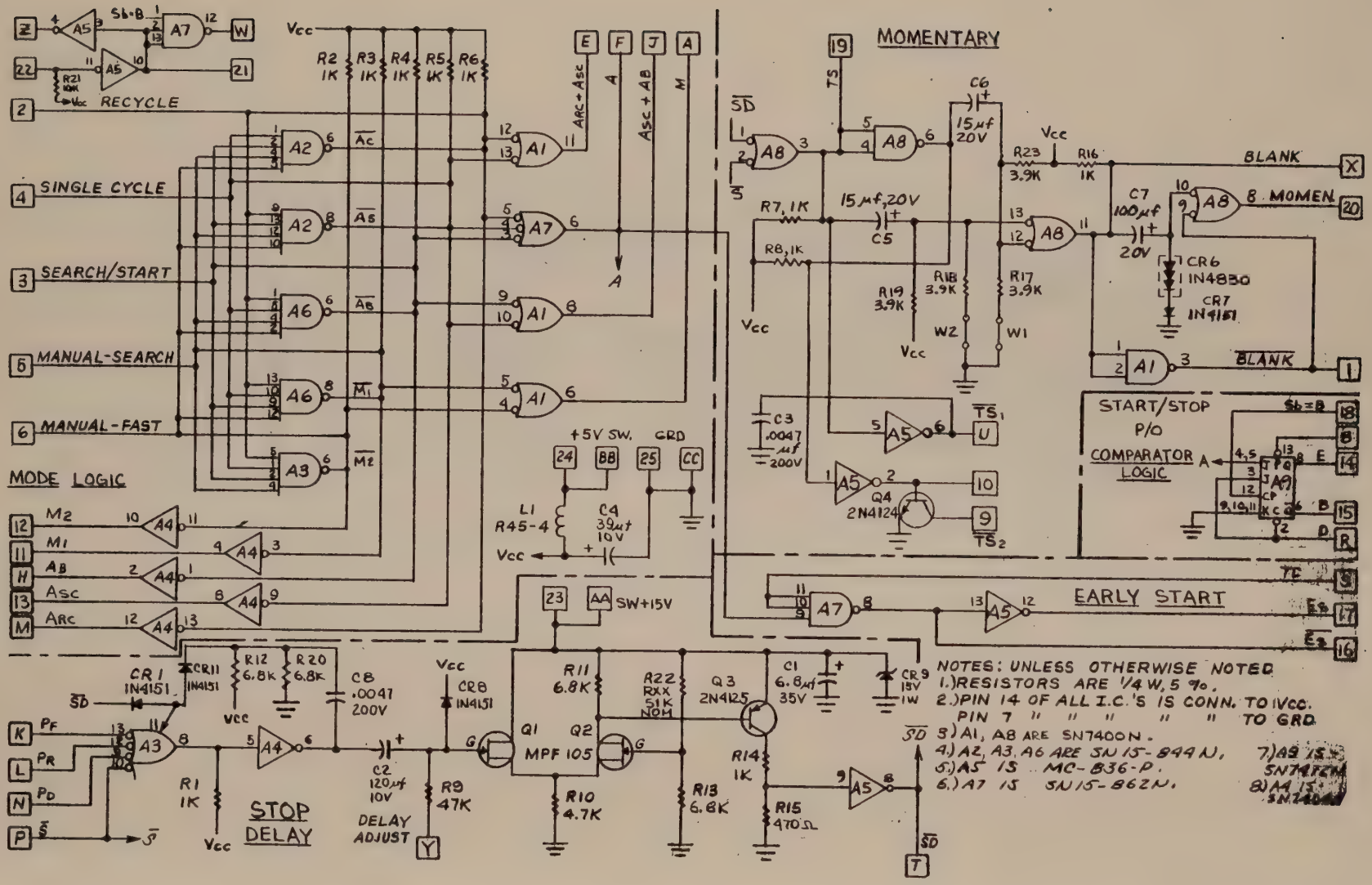
REF.	DESCRIPTION	SD PART NO.
	Assembly	021512-4-1
	Schematic	021512-7-3
A1,2,7,8	Integrated Circuit, SN15-844N	019714
A3,4	Integrated Circuit, SN15-832N	019713
A5	Integrated Circuit, MC836P	025704
A6	Integrated Circuit, SN7474N	025241
A9,10	Integrated Circuit, SN7402N	025709
C2,3	Capacitor, .1 µF, 10 V	100120
C4	Capacitor, 1 µF, 10 V	100082
C5	Capacitor, 47 pF, DM	100171
C6	Capacitor, 39 µF, 10 V, Tant	100183
CR1-11	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1	Transistor, 2N3904	101377
R1-3,5,9-13	Resistor, 1 k, 1/4 W, 5%, CC	101569
R4	Resistor, 4.7 k, 1/4 W, 5%, CC	101598
R6	Resistor, 100 k, 1/4 W, 5%, CC	101558
R7,8	Resistor, 10 k, 1/4 W, 5%, CC	101570
W1	Jumper, Molded	102879
W4	Jumper, #24 AWG	
	Extractors	100865

CIRCUIT DESCRIPTION
MODE LOGIC
SCHEMATIC #021513-7-1

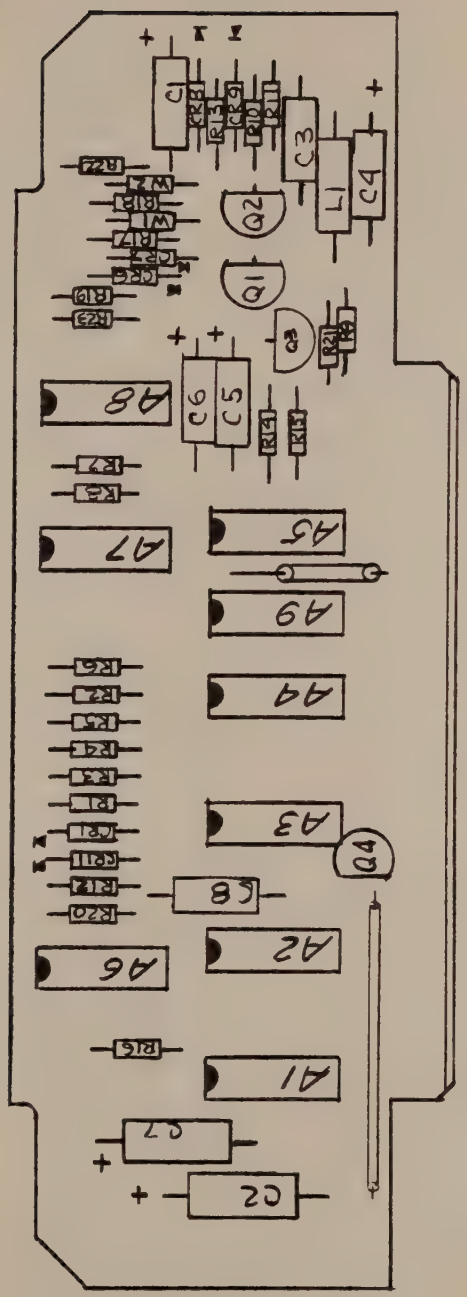
1) GENERAL

The Mode Logic card is one of a group of three cards which contain the comparator and control logic circuitry. The other two are the Comparator Logic card A23 and the Function Logic card A25. The functional descriptions of the circuitry on these two cards are provided in Sections 5.4.1 and 5.4.2.

The Mode Logic card contains the Mode Logic, the Stop Delay circuit, the Momentary circuit and part of the Comparator Logic.



MODE LOGIC SCHEMATIC #021513-7-1 REV K



MODE LOGIC ASSEMBLY #021513-4-1F

PARTS LIST

MODE LOGIC P.C. BOARD #021513-7-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021513-4-1
	Schematic	021513-7-1
	Mode P. C. Board	021513-1
A1,8	Integrated Circuit, SN7400N	019705
A2,3,6	Integrated Circuit, SN15-844N	019714
A4	Integrated Circuit, SN7404N	025779
A5	Integrated Circuit, MC-836P	025704
A7	Integrated Circuit, SN15-862N	019719
A9	Integrated Circuit, SN7472N	019967
C1	Capacitor, 6.8 µF, 35 V	100182
C2	Capacitor, 120 µF, 10 V	100206
C3,8	Capacitor, .0047 µF, 200 V	100129
C4	Capacitor, 39 µF, 10 V	100183
C5,6	Capacitor, 15 µF, 20 V	100211
C7	Capacitor, 100 µF, 20 V	100208
CR1,7,8,11	Diode, 1N4151	100385
CR6	Diode, 1N4830	100440
CR9	Diode, Zener, 1N4744A 15 V, 1 W	100422
L1	Inductor, R45-4	101313
Q1,2	Transistor, 2N5459	101384
Q3	Transistor, 2N3906	101378
Q4	Transistor, 2N3904	101377
R1-8,14,16	Resistor, 1 k, 1/4 W, 5%	101569
R9	Resistor, 47 k, 1/4 W, 5%	101574
R10	Resistor, 4.7 k, 1/4 W, 5%	101598
R11-13,20	Resistor, 6.8 k, 1/4 W, 5%	101544
R15	Resistor, 470 Ω, 1/4 W, 5%	101625
R17-19,23	Resistor, 3.9 k, 1/4 W, 5%	101601
R21	Resistor, 10 k, 1/4 W, 5%	101570
R22	Resistor, 51 k, 1/4 W, 5%	101590
W1,2	Jumper, Molded	102879
	Extractors	100865

CIRCUIT DESCRIPTION
DRIVERS
SCHEMATIC #021515-7-1

1) GENERAL

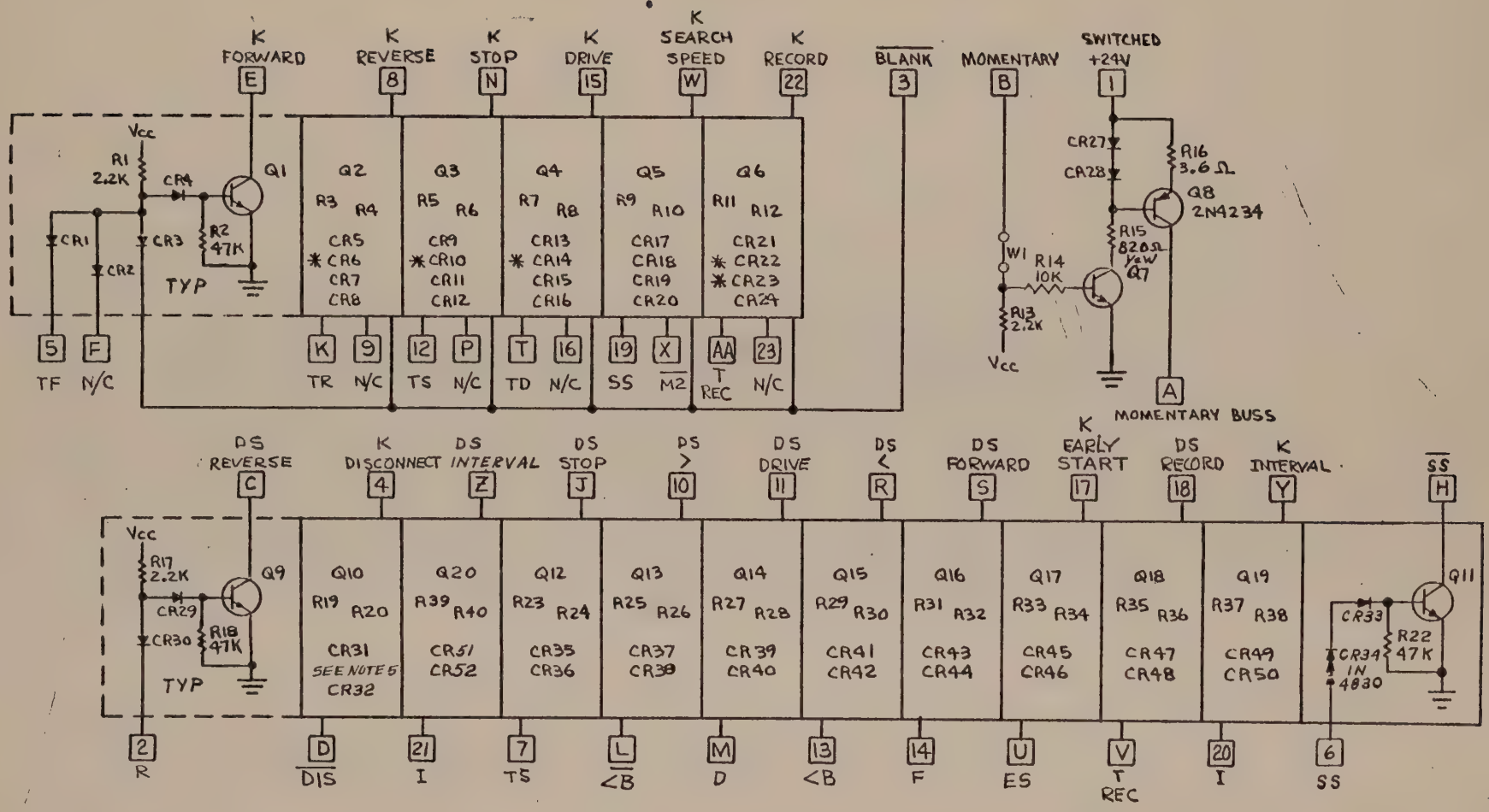
The Drivers Board contains the relay and lamp drivers. In addition, it includes the Momentary Bus drive circuit.

The transport control relays, (Forward, Reverse, Stop, Drive, and Search Speed) are driven from the first five circuits, Q1 through Q5. Each of these circuits is structured as a three-input NAND gate with one of the inputs to each circuit tied to the BLANK input from pin 3.

The Disconnect relay, the functional control switch lamps (Reverse Stop, Drive, and Forward), the time code status lamps (">", "<", and INTernal), and the SEARCH SPEED line used with Filter Option S13 are driven from circuits Q9 through Q20. With the exception of the SEARCH SPEED drive, Q11, these circuits are one-input versions of the first six.

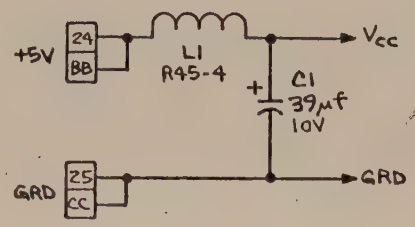
The Momentary Bus drive is from circuit Q7 and Q8. This circuit amplifies the MOMEN signal and feeds it to the Relay Assembly.

Sections 5.4.1 and 5.4.2 contain additional information on the functional operation of the driver circuits.

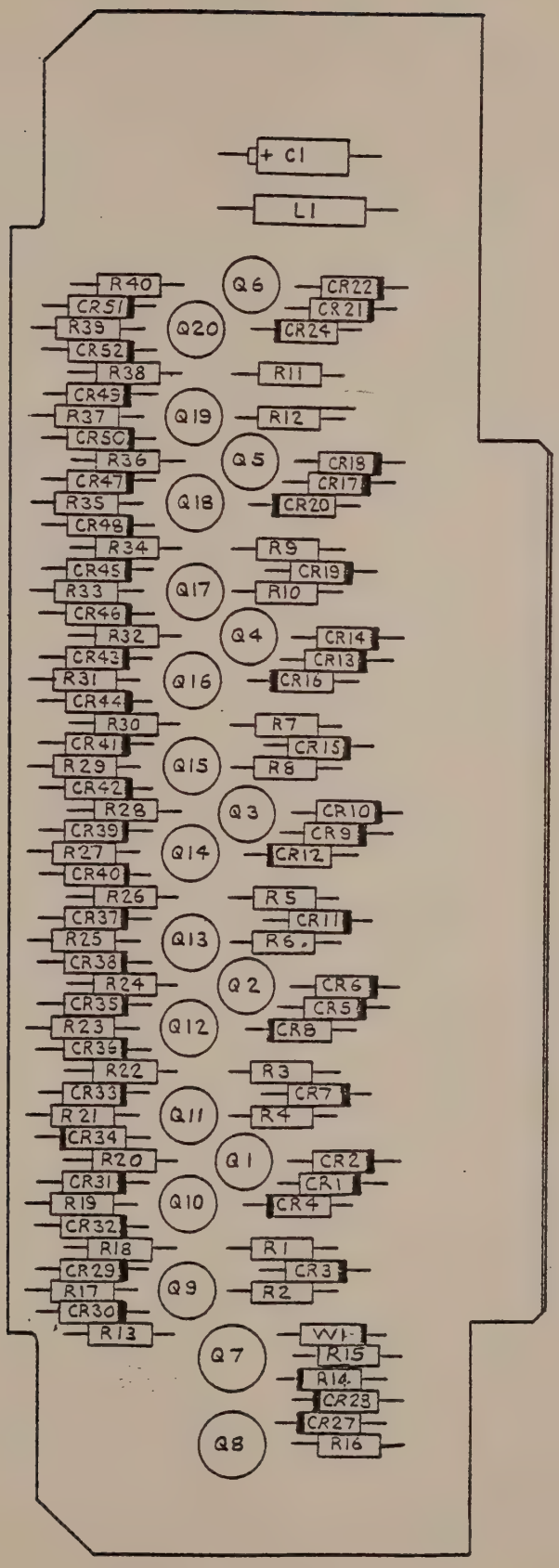


NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE 1/4W., 5%.
2. DIODES ARE IN4151.
3. TRANSISTORS ARE 2N2222.
4. * INDIACATES COMPONENTS NOT USED ON G1 ASSEMBLY.
5. CR31 ON G1 IS IN4829.



DRIVER SCHEMATIC #021515-7-1 (REV G)



DRIVER ASSEMBLY #021515-4-1 (REV J)

PARTS LIST

DRIVER #021515-7-1 REV G_n

REF.	DESCRIPTION	SD PART NO.
	Assembly	021515-4-1
	Schematic	021515-7-1
C1	Capacitor, 39 µF, 10 V	100183
CR1-5,7-9,11-13, 15-21,24,27-30, 32,33,35-52	Diode, 1N4151	100385
CR31	Diode, 1N4829	100443
CR34	Diode, 1N4830	100440
L1	Inductor, R45-4	101313
Q1-7,9-20	Transistor, 2N2222	101347
Q8	Transistor, 2N4234	101397
R1,3,5,7,9,11, 17,19,23,25,27, 29,31,33,35,37,39	Resistor, 2.2 k, 5%, ¼ W, CC	101562
R2,4,6,8,10,12, 20,22,24,26,28, 30,32,34,36,38,40	Resistor, 47 k, 5%, ¼ W, CC	101574
R14	Resistor, 10 k, 5%, ¼ W, CC	101570
R15	Resistor, 820 Ω, 5%, ½ W, CC	101656
R16	Resistor, 3.6 Ω, 5%, ¼ W, CC	101795
W1	Jumper, Molded	102879
	Pad, Transistor Mounting (Q8)	100666
	Extractor	100865

CIRCUIT DESCRIPTION
TIME-OF-DAY ACCUMULATOR
SCHEMATIC #021543-7-3

1) GENERAL

This card successively divides the 1 pps signal to provide outputs which represent seconds through hours. All outputs are buffered, an input inhibit circuit is provided, and the hours dividers are recycled at 23:59:59.

2) DIVIDERS

Dividers U9, U11, U13 and U14 are divide-by-10 circuits. Dividers U10 and U12 are divide-by-6 circuits. Each divider has its data inputs connected to a preset time source. Grounding the appropriate preset line will load the preset time into divider. Inverters U15 are used to buffer the seconds reset lines.

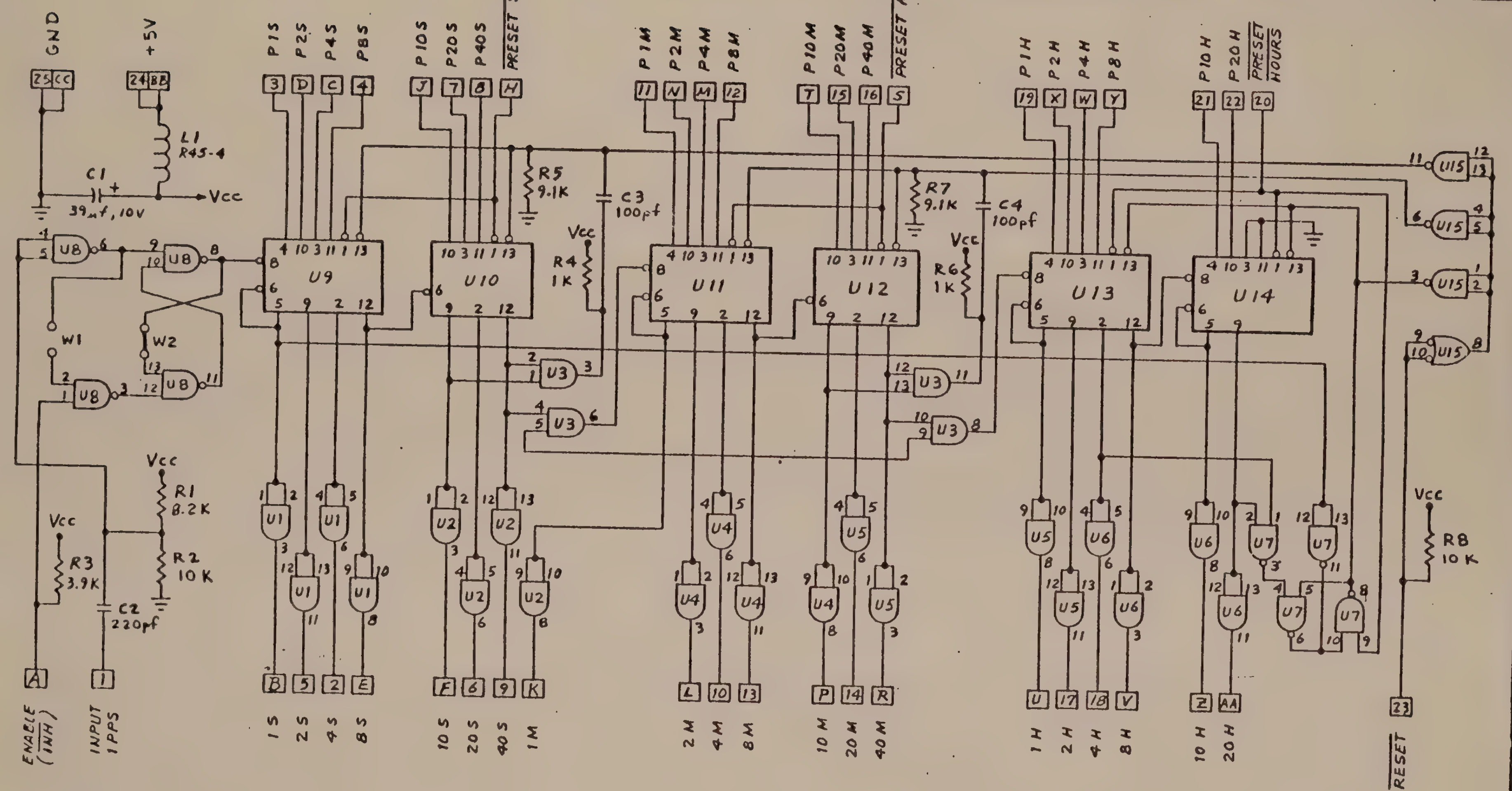
3) INHIBIT CIRCUIT

The inhibit circuit is used to stop updating of the accumulator when the front panel MODE switch is in the HOLD position, if present. Gate U8-6 inverts the 1 pps input. Gates U8-11/U8-8 form an RS flip-flop. Gate U8-3 inverts the INHIBIT/ENABLE line, pin A, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the INHIBIT/ENABLE line.

4) RECYCLE CIRCUIT

Gates U7-6/U7-8 are connected as an RS flip-flop to control the reset lines of dividers U13 and U14 for recycle at 23:59:59. Gate U7-3 NANDS the 20 hour and the 4 hour outputs to provide a low output at 24 hours. The flip-flop (U7-6/U7-8) output will also go low, resetting U13 and U14 at this time, provided the PRESET HOURS line is high. In this way, recycle is inhibited during preset. Gate U7-11 is wire AND-connected to the flip-flop and maintains the reset pulse for one second. This allows all the flip-flops in the dividers time to reset. Reset may also be initiated from the RESET line via U15-3.

REV	DESCRIPTION		ECO NO		
C	SEE ECO 13944.		13944		
C1	CHECKOUT EVALUATION		NFC		



NOTES

1. RESISTORS ARE ¼W, ±5%, CARBON COMPOSITION.
2. I.C.'s:

	TYPE	GND	Vcc
U1,2,3,4,5,6	MC 1806 P	7	14
U7, 8, 15	MC 846 P	7	14
U9,11,13,14	SN74 196N	7	14
U10,12	SN74LS197N	7	14

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ITEM NO	QTY	PART NUMBER	DESCRIPTION

LIST OF MATERIALS

DRAWN 3/13/80 · CHECK · ELECT. · MECH. · PROJECT 3/ /80 · QA

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±

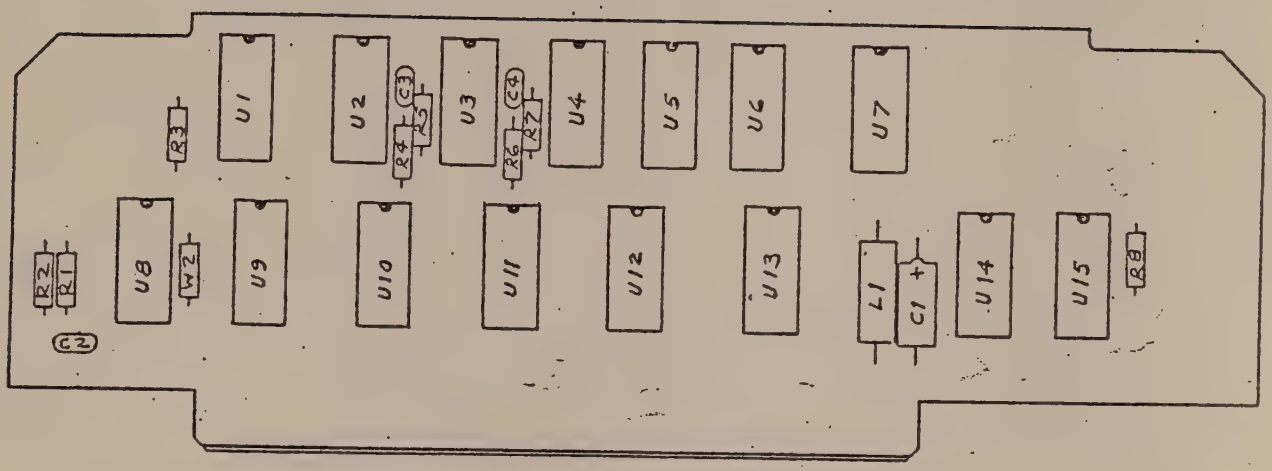
USED ON · NEXT ASSY · APPLICATION · SCALE · DO NOT SCALE

SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA
CODE IDENT. 52542

MATERIAL

ACCUMULATOR P.C. BOARD SCHEMATIC

DRAWING NO · REV



TIME-OF-DAY ACCUMULATOR ASSEMBLY #021543-4-3 REV B

PARTS LIST

TIME-OF-DAY ACCUMULATOR #021543-7-3

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021543-4-3
	Schematic	021543-7-3
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF	117633
C3-4	Capacitor, 100 pF	117628
L1	Inductor, R45-4	101313
R1	Resistor, 8.2 k 5%, 1/4 W	10159501
R2,8	Resistor, 10 k 5%, 1/4 W	10157001
R3	Resistor, 3.9 k 5%, 1/4 W	10160101
R4,6	Resistor, 1 k 5%, 1/4 W	10156901
R5,7	Resistor, 9.1 k 5%, 1/4 W	10157301
U1-6	Integrated Circuit, MC1806P	025733
U7-8,15	Integrated Circuit, MC846P	019716
U9,11,13-14	Integrated Circuit, SN74196N	025784
U10,12	Integrated Circuit, SN74LS197N	103165
W2	Jumper, Molded	102879

CIRCUIT DESCRIPTION
CODE GENERATOR
SCHEMATIC #021554-7-1

1) GENERAL

The IRIG DC Code Generator card can be used to generate the IRIG A, B, C, E, or H codes. Code selection may be remotely controlled or fixed by the particular card configuration. Days information may be optionally included and provision is made for the insertion of control function bits and/or straight binary seconds from a source external to the card. The following description is intended to apply in general to all configurations of the card. The specific assembly used is identified by the attached assembly, schematic and parts list.

2) DIVIDER CIRCUITS

Refer to the timing diagrams and the schematic for this and subsequent sections. Divider A8 is a divide-by-two, then-by-five counter which divides down the "Z" RATE" and provides decoded outputs for the code generating gates. Divider A15 is a divide-by-five, then-by-two counter which takes the output of A8, divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A17 is a divide-by-two, then-by-six counter. Its principle function is to control the secondary scan gate A4. The divide-by-twelve is used only for IRIG C, the divider being reset at the count of ten or by the sync input for the other codes. This early reset is shown on the timing diagram as A18-8. The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on Sheet two is simply eliminated when the divider resets at ten. Reset at ten is established by gate A18-8. A one-shot (A18-12,6) performs code frame reset. The external reset signal (pin Z) may be used for code frame reset when W1 is installed, or the card can supply a reset pulse to synchronize the associated accumulator when W2 is installed.

Divider A7 (if present) is a divide-by-five counter provided for external use. It is synchronized with the other divider chips.

3) SCAN GATES

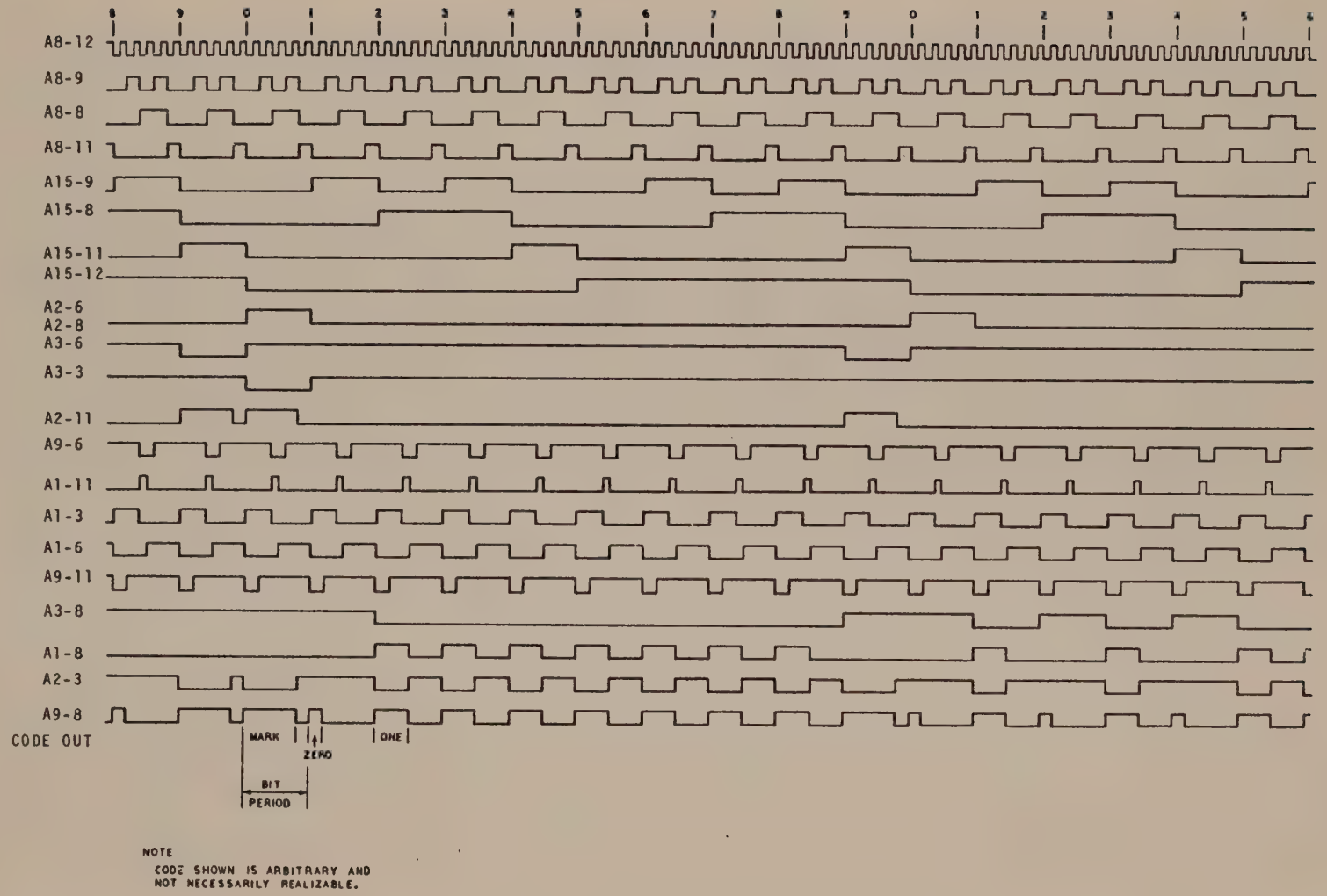
Creation of serial ONES is accomplished by a two-stage switching network and a series of gates. Chips A10-A14 are basically single pole (pin 8 is the output), 8-position switches. The inputs to these switches are the time data from the system accumulator. (One or more of these chips may be deleted on a particular card configuration.) The switching is controlled by BCD information on pins 1, 2 and 13. Since the above switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus, the need for

switch A4. This switch, controlled from the BCD outputs of divider A17, selects the proper time interval for serializing each switch output. (The series of gates associated with A14 and A13, if present, further control these switches which may have outputs that should not be present in certain codes.) For example, tenths-of-seconds are added only in IRIG A, units-of-seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A5-8, A5-11 and A3-8 are used to inhibit the presence of serials ONES at certain times when no serial ONES should be present. This prevents the spurious ONES (coming from the switches) from appearing in the output code.

4) CODE GENERATING GATES

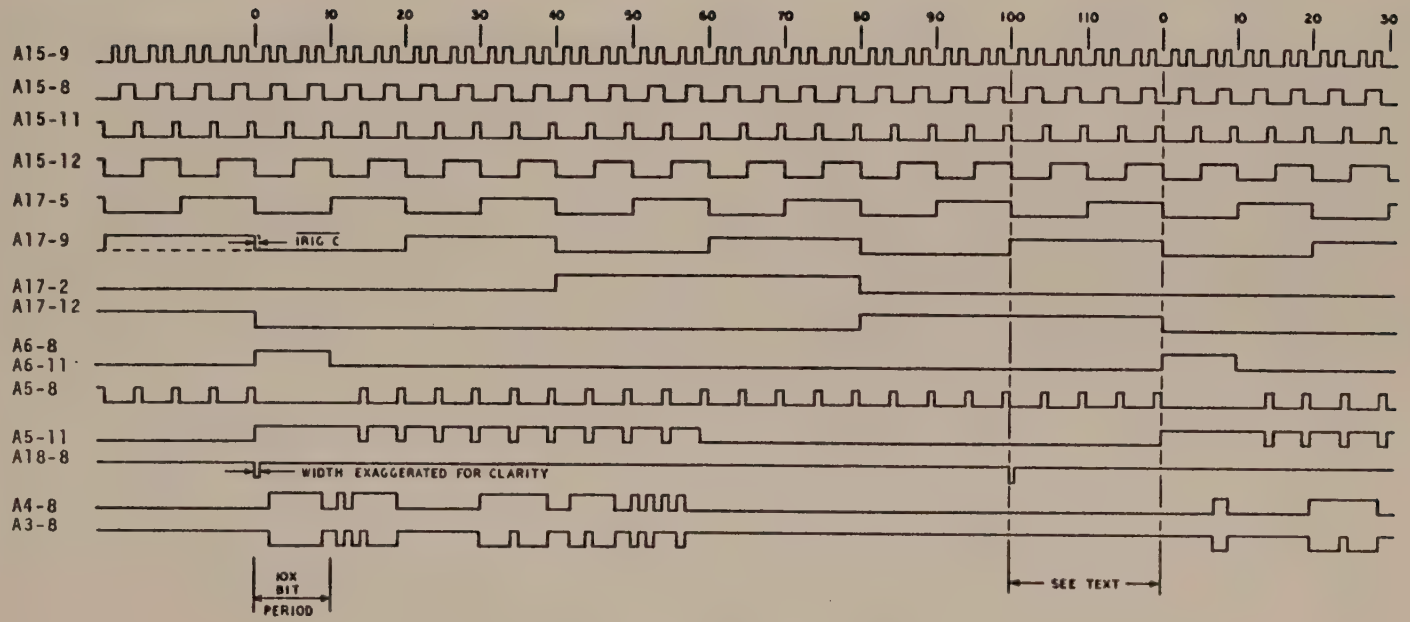
These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin 2. A "2" length is a ZERO, a "5" is a ONE, and an "8" is an INDEX MARKER.

The INDEX MARKERS are generated by gating the output of divider A15. Gate A1-3 adds information from the output of divider A11 to create the "8" width. Gates A6-8 and A6-11 allow an extra pulse from gates A2-6 and A2-8 to give the "double mark" at the start of the frame. Gate A3-6 provides the marker at each tenth frame interval. Gate A9-11 supplies a pulse of "2" width at the start of each bit interval. If a MARKER or a ONE is not present, then the output code will be high for only the "2" width. Gate A1-6 supplies the "5" width pulse. This is AND-gated with the $\overline{\text{SERIAL ONES}}$ from A3-8 by gate A1-8. (External bits may be inserted on this same line through pin 22.) The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A2-3 and A9-8 are used to combine the various widths to produce the output code at pin B.



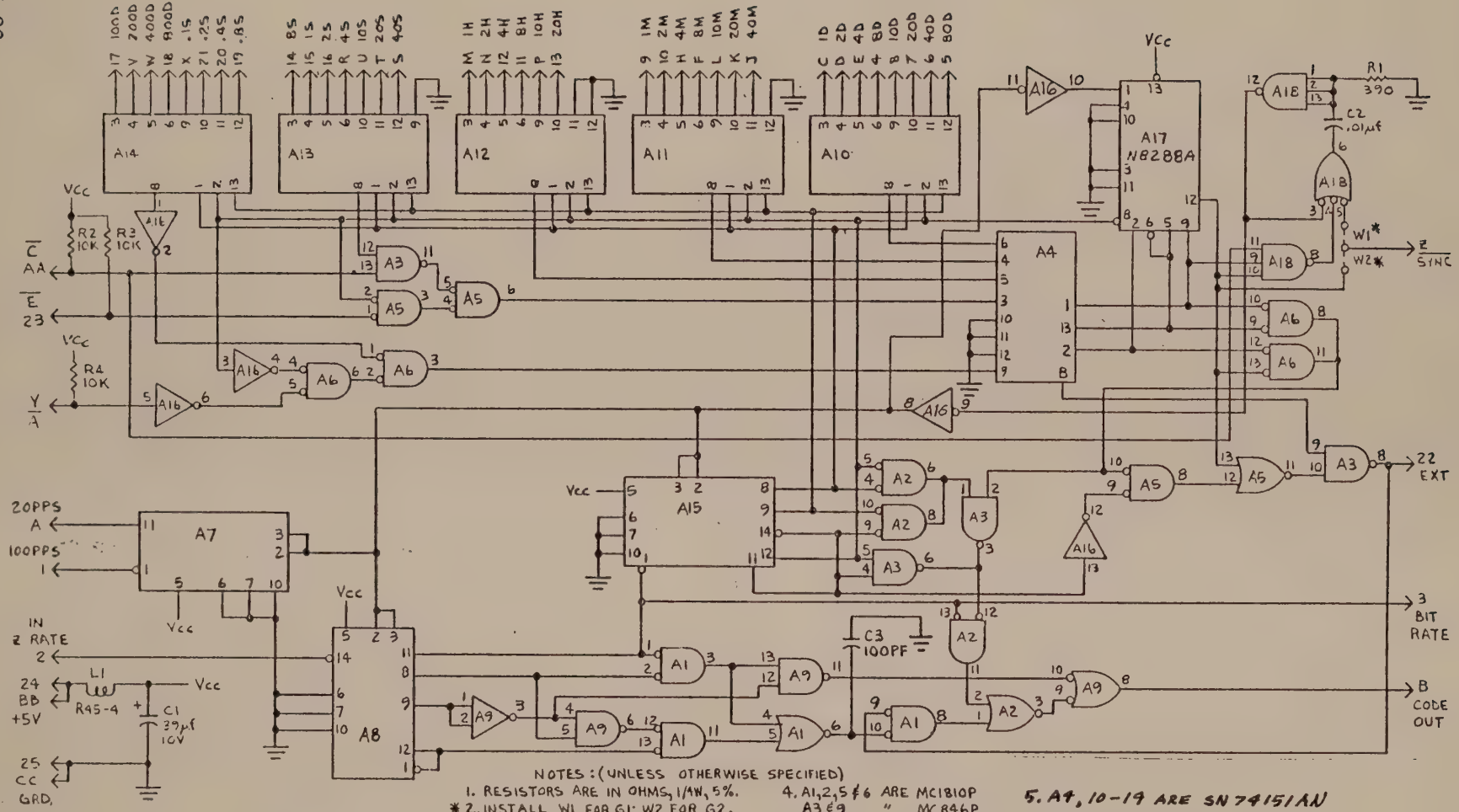
NOTE
CODE SHOWN IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 1 of 2)



NOTE:
CODE SHOWN (SERIAL ONES & A18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

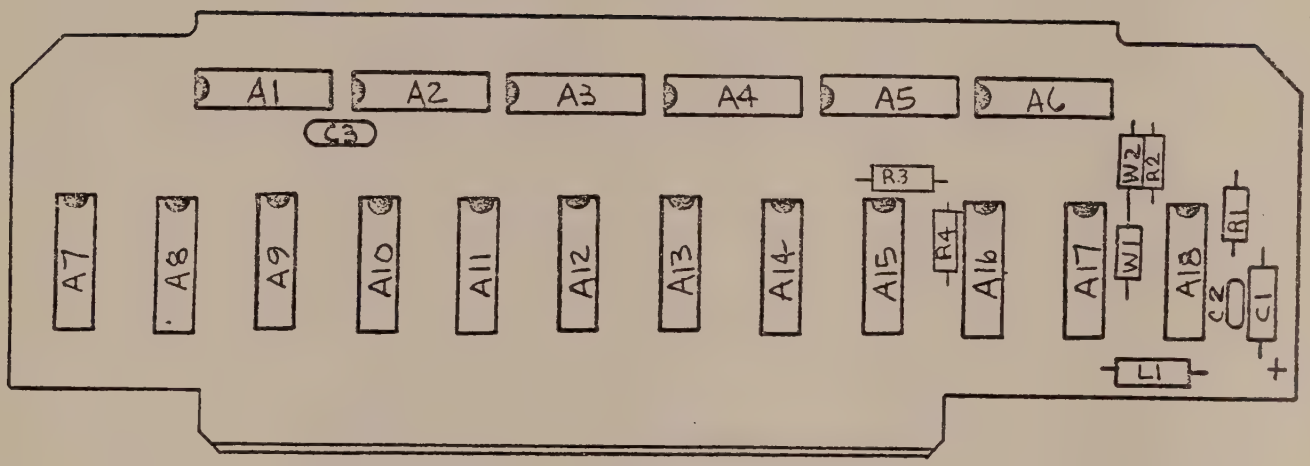
IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 2 of 2)



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
* 2. INSTALL W1 FOR G1; W2 FOR G2.
3. PIN 7 OF ALL IC'S. IS CONN. TO GRD.
" 14 " " " " " " Vcc
4. A1,2,5 & 6 ARE MC1810P
A3 & 9 " MC846P
A16 IS MC836P
A18 " SN7410N
5. A4, 10-19 ARE SN74151AN PIN 8 GND, PIN 16 Vcc.
6. A7, 8, 15 ARE SN7490N.

IRIG A-B-C-E SWITCHABLE DC CODE GENERATOR SCHEMATIC #021554-7-1 REV E



CODE GENERATOR ASSEMBLY #021554-4-1 REV C

PARTS LIST

CODE GENERATOR ASSEMBLY #021554-4-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021554-4-1
	Schematic	021554-7-1
A1,2,5,6	Integrated Circuit, MC1810P	025735
A3,9	Integrated Circuit, MC846P	019716
A4,10-14	Integrated Circuit, SN74151AN	02577101
A7,8,15	Integrated Circuit, SN7490N	025732
A16	Integrated Circuit, MC836P	025704
A17	Integrated Circuit, N8288A	025723
A18	Integrated Circuit, SN7410N	019706
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, .01 µF, 100 V	100103
C3	Capacitor, 100 pF, 500 V	100173
L1	Inductor, R45-4	101313
R1	Resistor, 390 Ω 5%, 1/4 W	101592
R2-4	Resistor, 10 k 5%, 1/4 W	101570
	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
MODULATOR
SCHEMATIC #021556-7-5

1) GENERAL

The Shaper and Modulator card can be assembled to provide up to three shaper circuits, a modulator, a dc code output buffer, a Days/ID control circuit, a square-wave decoder and miscellaneous inverters and buffers. The shaper circuits are identical with the exception that three capacitors within each circuit are a function of frequency. The following description is intended to apply to all card configurations. The specific assembly used is covered by the attached schematic, assembly and parts list.

2) SHAPERS

Each of the shaper circuits (up to three) are identical, with the exception that the values chosen for three capacitors in each circuit are inversely proportional to the resonant frequency. Each shaper accepts a logic level square wave at the selected carrier frequency and outputs an in-phase sine wave which may be selected (through switching external to the card) and fed to the modulator. The input is filtered and applied to the base of a constant-current amplifier which drives an active circuit having the electrical properties of a tuned tank circuit. A potentiometer is provided to adjust the resonant frequency. The sine wave output from this circuit is buffered and ac-coupled to output pin M, S or T.

3) MODULATOR

The modulator accepts the selected carrier sine wave at pin W and modulates it with the dc level shift code at pin F. The resulting modulated code is fed through amplifier A4 to output pin X.

A MODULATION RATIO adjustment, R16, sets the percentage of modulation before the signal is fed to A4. A MODULATED CODE AMPLITUDE adjustment, R20, determines the gain of amplifier A4, thus, establishing the signal level at pin X. (0 to 10 V p-p.)

4) DC CODE BUFFER

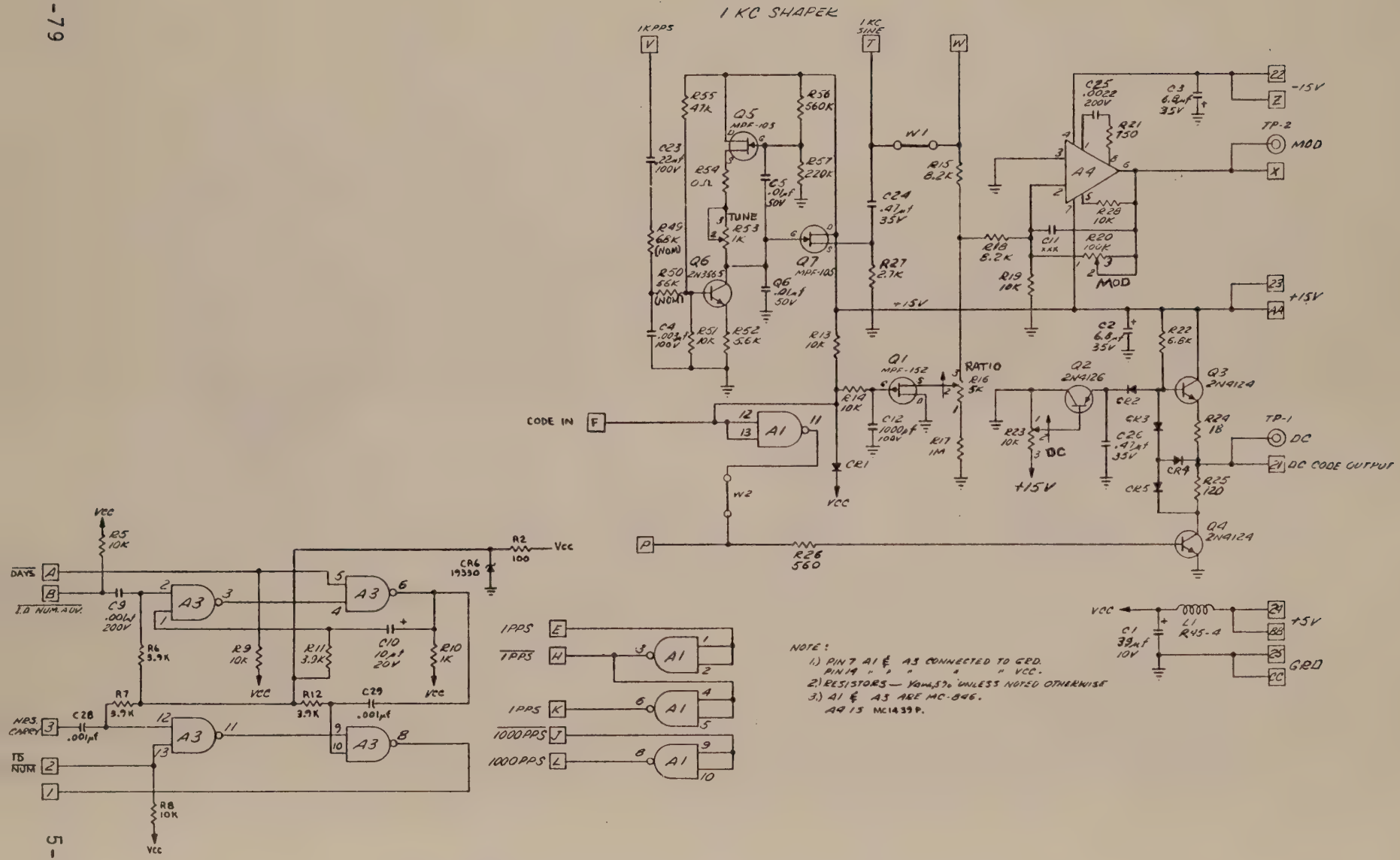
The dc level shift code input to pin F is inverted once by A1-11 and again by Q4 before being fed as the dc code output to pin 21, through R25. Transistors Q2 and Q3, and the DC CODE AMPLITUDE potentiometer R23 establish the output level at pin 21 (0.4 V to +10 V). Short-circuit protection is provided by CR3, CR4 and R24. The quiescent current in Q3 and Q4 is determined by CR3, CR5 and R25.

5) DAYS/ID (RUN NUMBER) CONTROL

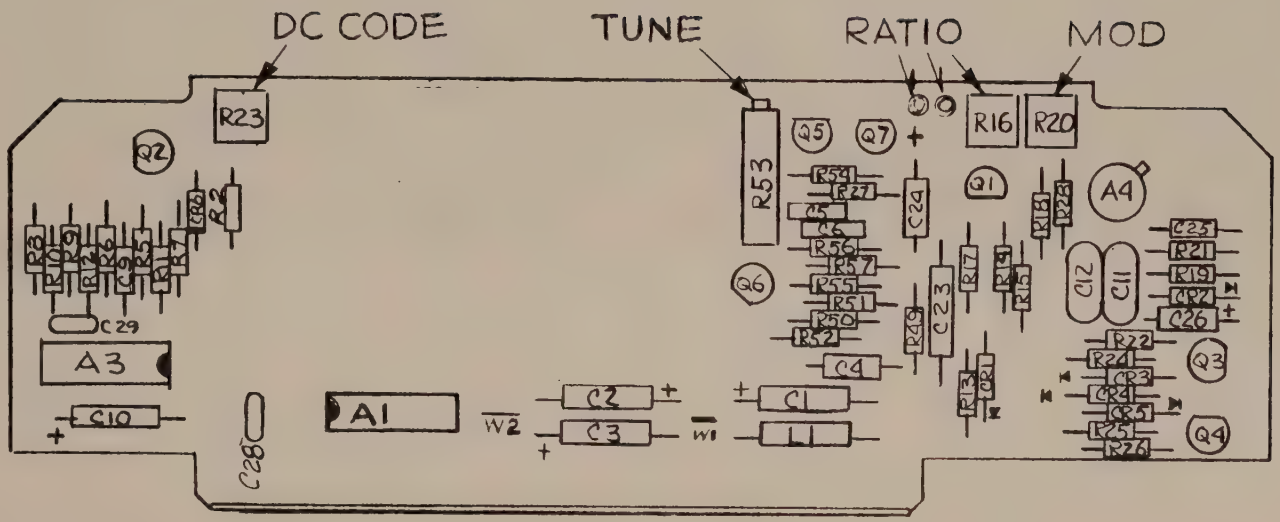
Gates on A3 control the selection of the signal which is used to update the days accumulator in the system. The carry output from the Time-of-Day Accumulator is inverted and applied to A3-9. If the other input (the $\overline{\text{IN NUM}}$ line) is high (i.e. left open), the hours accumulator carry signal will update the days accumulator. Similarly, a high on the $\overline{\text{DAYS}}$ line permits a signal on pin B ($\overline{\text{ID NUM ADV}}$) to update the days accumulator. The ID advance input pulses are standardized by one-shot A3-3,6 to ensure reliable operation.

6) BUFFERS

Extra gates on A1 are made available for external use as inverters and buffers.



SHAPER/MODULATOR SCHEMATIC #021556-7-5 REV D



MODULATOR ASSEMBLY #021556-4-5 REV D

PARTS LIST

MODULATOR #021556-7-5

REF.	DESCRIPTION	SD PART NO.
	Assembly	021556-4-5
	Schematic	021556-7-5
A1,3	Integrated Circuit, MC846P	019716
A4	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 6.8 µF, 35 V	100182
C4	Capacitor, 3300 pF, 100 V, Mylar	100153
C5,6	Capacitor, .01 µF, 50 V	100132
C9	Capacitor, 1000 pF, 200 V, Mylar	100137
C10	Capacitor, 10 µF, 20 V, Tant	100063
C11	Capacitor, Selected	CXXXXX
C12	Capacitor, 1000 pF, 100 V, DM	100243
C23	Capacitor, .22 µF, 100 V	100148
C24,26	Capacitor, .47 µF, 35 V, Tant	100140
C25	Capacitor, 2200 pF, 200 V, Mylar	100185
C28,29	Capacitor, 1000 pF, Disc	100076
CR1-5	Diode, 1N4151	100385
CR6	Diode, 19330	019330
L1	Inductor, R45-4	101313
Q1	Transistor, 2N5461 (MPF-152)	101383
Q2	Transistor, 2N3906	101378
Q3,4	Transistor, 2N3904	101377
Q5,7	Transistor, 2N5459 (MPF-105)	101384
Q6	Transistor, 2N3565	101371
R2	Resistor, 100 Ω, 5%, 1/4 W, CC	101609
R5,8,9,13,14, 19,28,51	Resistor, 10 k, 5%, 1/4 W, CC	101570
R6,7,11,12	Resistor, 3.9 k, 5%, 1/4 W, CC	101601
R10	Resistor, 1 k, 5%, 1/4 W, CC	101569
R15,18	Resistor, 8.2 k, 5%, 1/4 W, CC	101595
R16	Resistor, 5 k, 62 PA, Var	101845
R17	Resistor, 1 M, 5%, 1/4 W, CC	101605
R20	Resistor, 100 k, 62 PA, Var	101934
R21	Resistor, 750 Ω, 5%, 1/4 W, CC	101689
R22	Resistor, 6.8 k, 5%, 1/4 W, CC	101544
R23	Resistor, 10 k, 62 PA, Var	101937

PARTS LIST
MODULATOR #021556-7-5 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R24	Resistor, 18 Ω, 5%, 1/4 W, CC	101727
R25	Resistor, 120 Ω, 5%, 1/4 W, CC	101717
R26	Resistor, 560 Ω, 5%, 1/4 W, CC	101583
R27	Resistor, 2.7 k, 5%, 1/4 W, CC	101599
R49	Resistor, 68 k, 5%, 1/4 W, CC	101597
R50	Resistor, 56 k, 5%, 1/4 W, CC	101670
R52	Resistor, 5.6 k, 5%, 1/4 W, CC	101584
R53	Resistor, 1 k, Beck. 79P, Var	102181
R54,W1,2	Wire, Insulated #24	
R55	Resistor, 47 k, 5%, 1/4 W, CC	101574
R56	Resistor, 560 k, 5%, 1/4 W, CC	101687
R57	Resistor, 220 k, 5%, 1/4 W, CC	101610
	Extractor	100865

CIRCUIT DESCRIPTION
TIME BASE/SERIAL PRESET-RESET
SCHEMATIC #021566-7-11

1) GENERAL

The Time Base/Serial Preset-Reset Card contains the time base circuitry and two identical circuits for independent preset of the TOD and Days Accumulators.

2) TIME BASE

The Time Base section consists of an unheated crystal, Y1, and feedback amplifier Q1. The oscillator output, at pin Y, may be utilized as an external reference or it may be jumpered to pin W for internal use on the card. An external reference signal may be utilized by applying it to pin W in place of the above signal.

The time base signal is applied to the base of voltage-amplifier Q2 (which has a gain of three), isolated, then fed to the base of Q3. Clipper-circuit Q3 provides a 5 V p-p square wave at pin X.

3) DIVIDER CHAIN

Control gate A5-6 receives the output of Q3 or the external reference via pin 13 depending upon which is selected.

The time base pulse rate at this point is 1 Mpps. Control gate A5-6 has two other inputs. One is the Elapsed Time input from pin 14 and the other is from Stop/Start flip-flop A4-5.

When a logic 0 (ground) is applied to the External Stop line (pin T), flip-flop A4-3 will generate a Logic 0 which will close gate A5-6 and inhibit the time base input to the divider chain. A positive transition on pin 11 or R, (the Stop time input) will also inhibit the time base if pin S is at ground.

A ground signal on the $\overline{\text{START}}$ pin 12 will set A4-5 and open gate A5-6.

The divider chain consists of three divider chips (A12, A13 and A6) connected in tandem. They divide the 1 Mpps time base down to 1 kpps. The first two (A12 and A13) are connected as divide-by-5, then-by-2 counters. These develop 100 kpps and 10 kpps square waves at pins 20 and 15, respectively. The third decade (A6) is connected in the normal divide-by-2, then-by-5 arrangement. BCD outputs (1-2-4-8) are provided at pins 21, U, V and 17. Flip-flop A4-9 develops complementary 1 kpps square wave outputs at pins 10 and 9.

Pin 2 is the zero reset input to A12. The zero reset inputs to A13 and A6 are connected to pin 19. These lines must be grounded if not in use.

4) PRESET OPERATION

Operations of the Time-of-Day Preset and Days Preset circuits are identical and only the Time-of-Day circuit will be described.

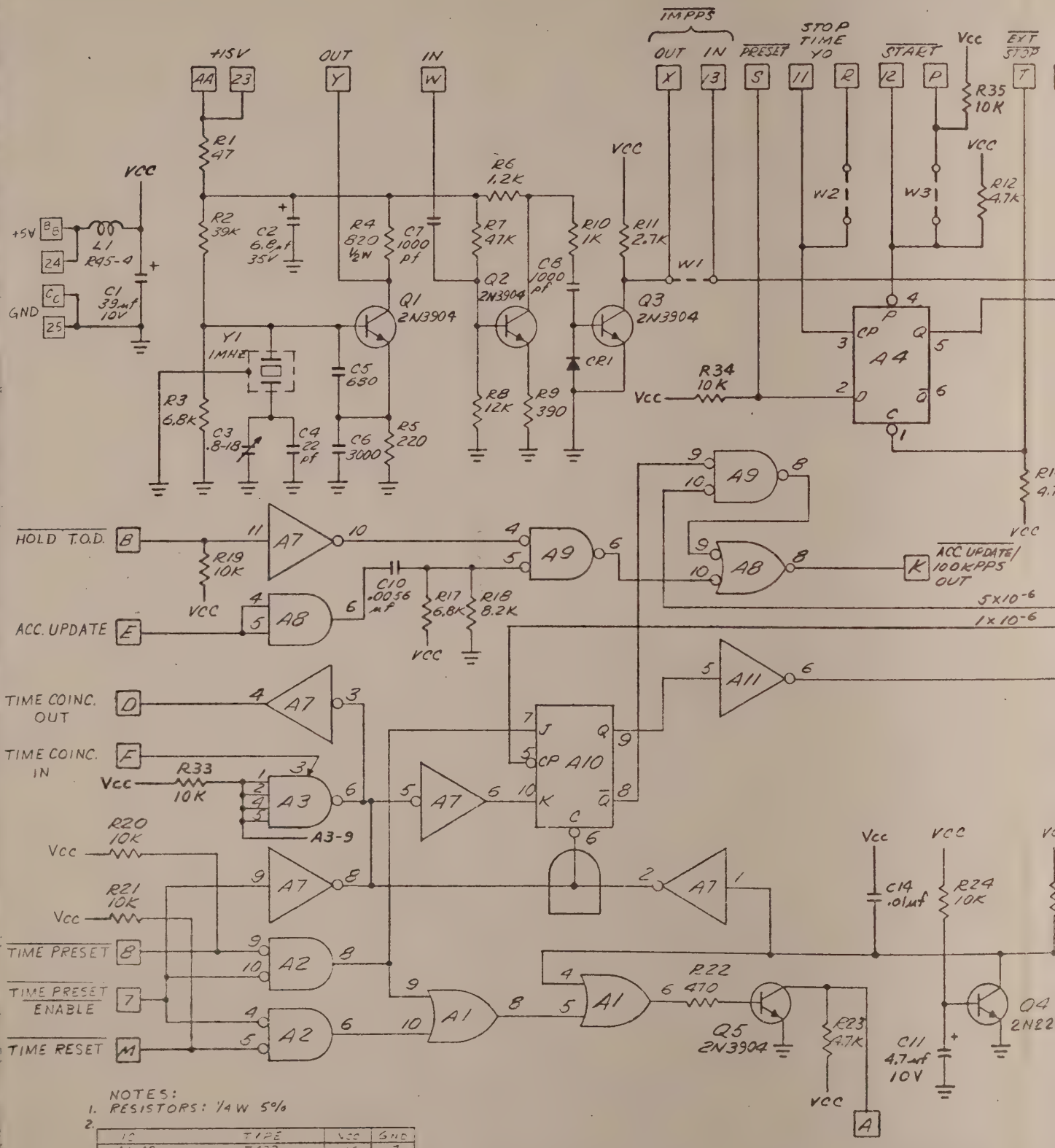
During normal operation of the Generator, the preset circuits connect the normal update inputs to their respective accumulators. In the case of the TOD Preset circuit this is the 1 pps input to pin E which is buffered by A8-6 then differentiated and fed to the TOD Accumulator through A9-6, A8-8 and pin K.

To initiate a TOD Preset cycle the $\overline{\text{Enable}}$ input to pin 7 must be at ground. (This condition exists in the PRESET position of the MODE Switch.) A ground on pin 7 opens gates A2-6 and A2-8 and removes the clear input to flip-flop A10-9 through inverter A7-8. The actual preset cycle is started when the PRESET/RESET Switch is momentarily thrown to the PRESET position grounding pin 8. The A2-8 output goes positive enabling the J input to flip-flop A10-9 and resetting the TOD Accumulator through A1-8, A1-6, Q5 and pin A. The next negative transition of the 500 kpps (1×10^{-6}) clock input sets flop-flop A10-9 and opens gate A9-8 to the 100 kpps (5×10^{-6}) pulse train feeding these signals to the TOD Accumulator update input through A8-8 and pin K.

The accumulator begins to update as soon as the PRESET/RESET Switch is opened removing the reset. The parallel BCD outputs from the TOD Accumulator are compared with the contents of the PRESET thumbwheel Switchs. At coincidence the signal TIME COINC goes high. The A3-6 output on the Time Base/Serial Preset Card goes low driving the K input to flip-flop A10-9 positive through inverter A7-6. Flip-flop A10-9 is cleared on the next negative transition of the 500 kpps clock closing gate A9-8. The TOD Accumulator is now set to the preset start time.

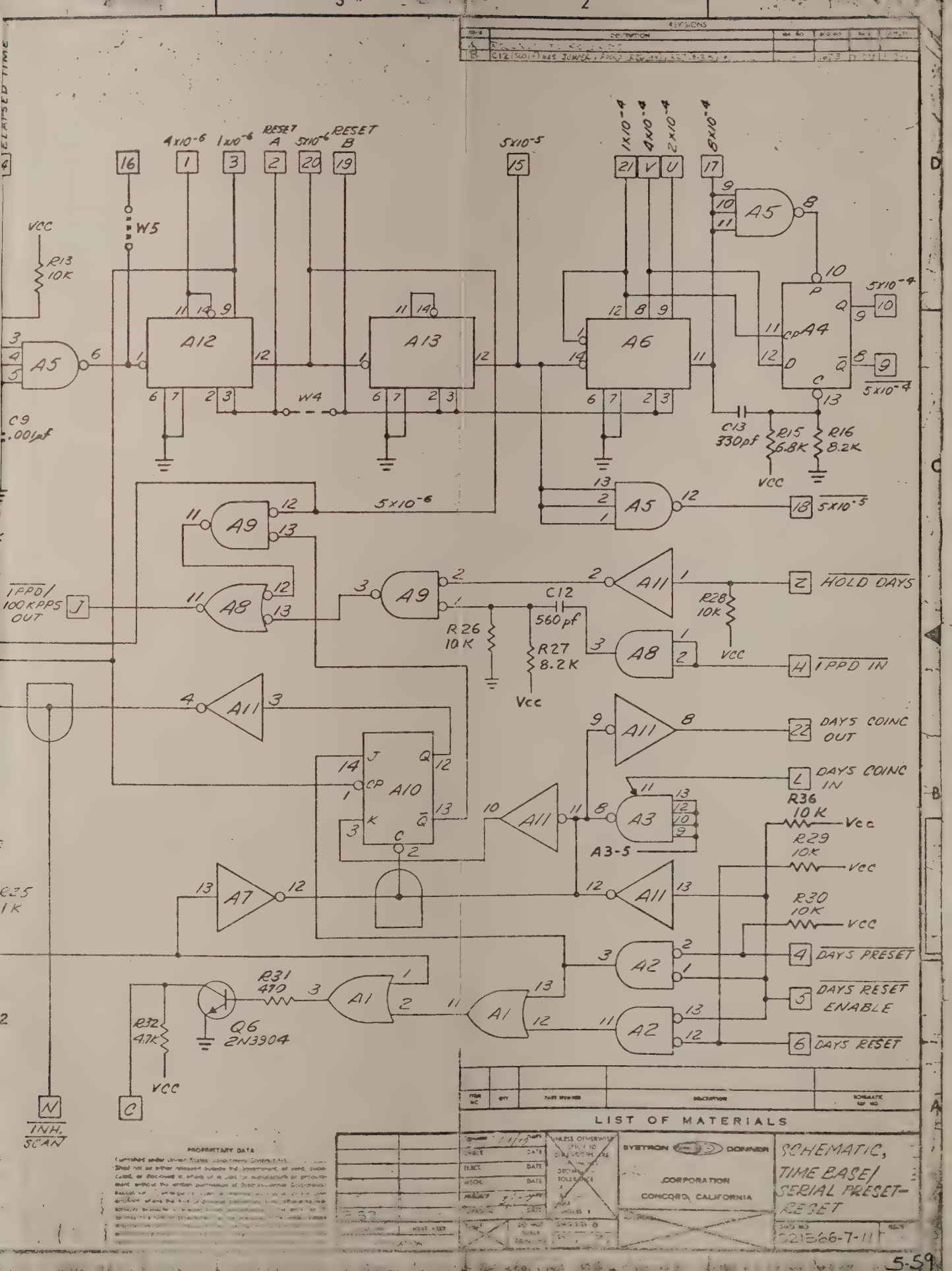
5) RESET OPERATION

The accumulator is reset to zero when power is first turned on in the system. This occures in the interval before capacitor C11 charges turning on Q4. The TOD Accumulaotr may also be reset when pin 7 is at ground by momentarily grounding pin M.

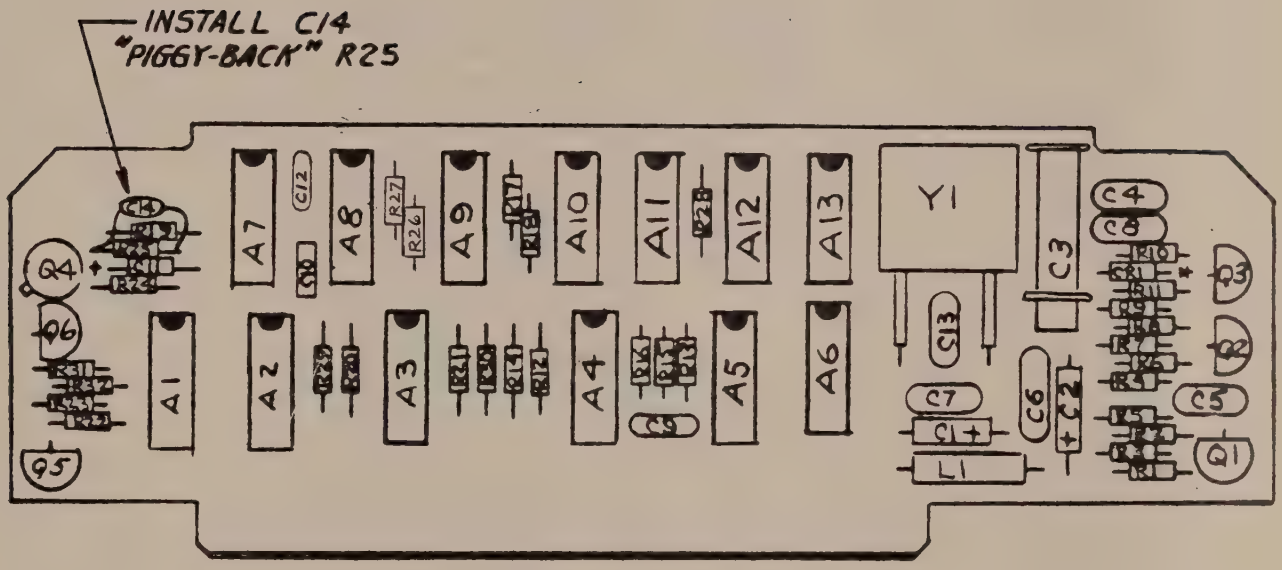


NOTES:
1. RESISTORS: ¼W 5%
2.

IC	TYPE	Vcc	GND
A1, A9	7432	14	7
A2	MC3002P	14	7
A3	1583Q	14	7
A4	7474	14	7
A5	7410	14	7
A6, 12, 13	7409	5	10
A7, 11	MC834P	14	7
A8	7408	4	7
A10	7473	4	11



REVISIONS
DESCRIPTION
ELAPSED TIME
4x10-6
1x10-6
RESET A
5x10-6
RESET B
5x10-5
1x10-4
4x10-4
2x10-4
8x10-4
W5
VCC
R13 10K
A5
A12
A13
A6
A4
W4
C9 .001µf
C13 330pf
R15 6.8K
R16 8.2K
5x10-4
5x10-5
A9
A8
A11
A10
A3
A7
A1
A2
1PPD/ 100KPPS OUT
HOLD DAYS
1PPD IN
DAYS COINC OUT
DAYS COINC IN
R26 10K
C12 560pf
R27 8.2K
R28 10K
R36 10K
R29 10K
R30 10K
A3-5
DAYS PRESET
DAYS RESET ENABLE
DAYS RESET
R31 470
R32 4.7K
Q6 2N3904
INH. SCAN
PROPRIETARY DATA
LIST OF MATERIALS
BYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
SCHEMATIC, TIME BASE/ SERIAL PRESET-RESET
021566-7-11



TIME BASE/SERIAL PRESET-RESET ASSEMBLY #021566-4-11

PARTS LIST

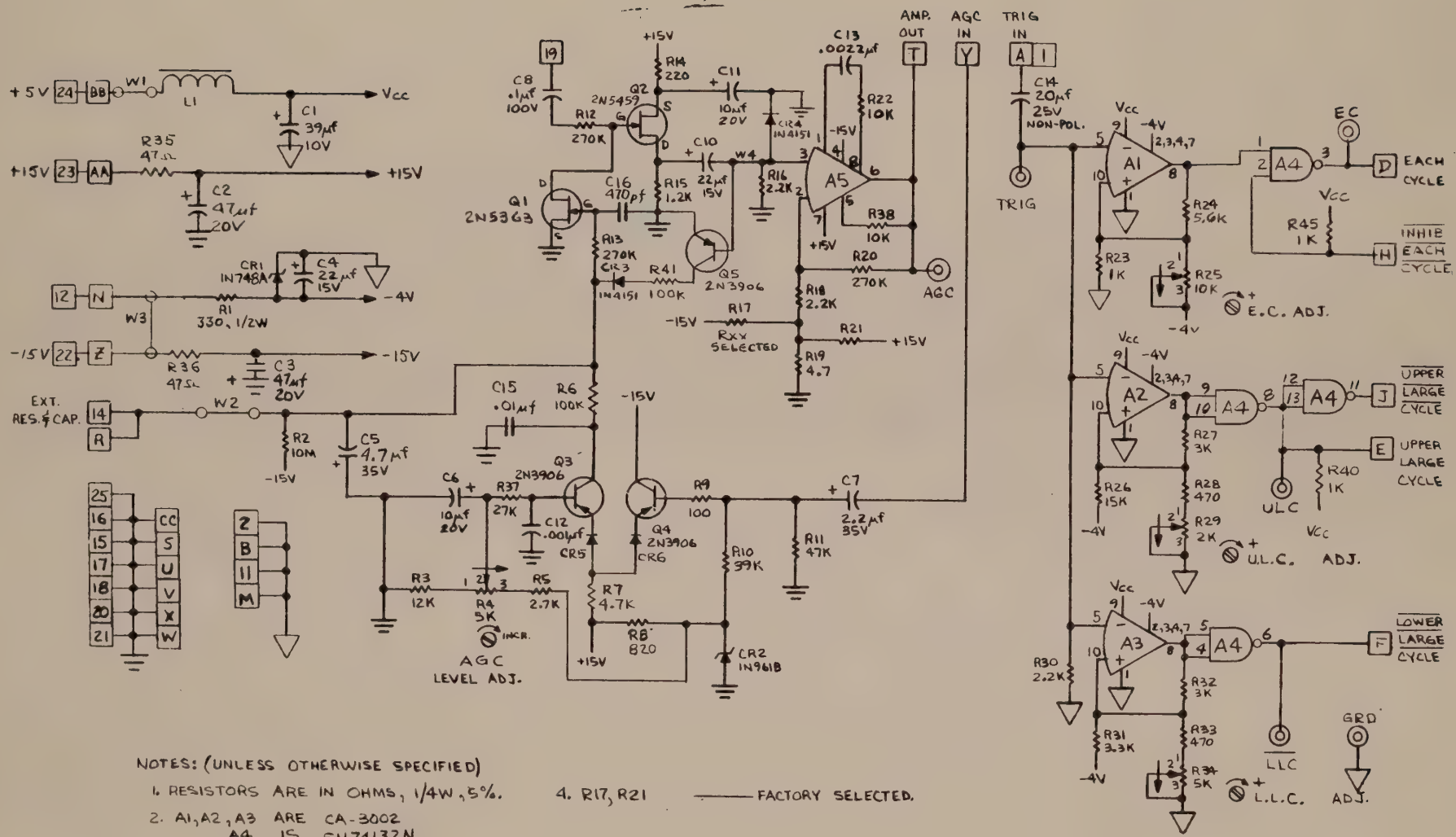
TIME BASE SERIAL PRESET/RESET #021566-7-11 REV B_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021566-4-11
	Schematic	021566-7-11
A1,9	Integrated Circuit, SN7432N	045257
A2	Integrated Circuit, MC3002P	025739
A3	Integrated Circuit, SN15830N	019712
A4	Integrated Circuit, SN7474N	025241
A5	Integrated Circuit, SN7410N	019706
A6-12,13	Integrated Circuit, SN7490N	025732
A7,11	Integrated Circuit, MC836P	025704
A8	Integrated Circuit, SN7408N	103093
A10	Integrated Circuit, SN7473N	019709
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 6.8 µF, 35 V	100182
C3	Capacitor, .8-18 pF, Variable	100102
C4	Capacitor, 22 pF	100068
C5	Capacitor, 680 pF	100275
C6	Capacitor, 3000 pF	100149
C7,8	Capacitor, 1000 pF	100243
C9	Capacitor, .001 µF	100076
C10	Capacitor, .0056 µF	116056
C11	Capacitor, 4.7 µF, 10 V	100205
C12	Capacitor, 560 pF, DM	100222
C13	Capacitor, 330 pF	100276
C14	Capacitor, .01 µF, Disc.	100103
CR1	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1-3,5,6	Transistor, 2N4124	101377
Q4	Transistor, 2N2222	101347
R1	Resistor, 47 Ω, 5%, ¼ W	101560
R2	Resistor, 39 k, 5%, ¼ W	101561
R3,15,17	Resistor, 6.8 k, 5%, ¼ W	101544
R4	Resistor, 820 Ω, 5%, ½ W	101656
R5	Resistor, 220 Ω, 5%, ¼ W	101566
R6	Resistor, 1.2 k, 5%, ¼ W	101581
R7	Resistor, 47 k, 5%, ¼ W	101574
R8	Resistor, 12 k, 5%, ¼ W	101565
R9	Resistor, 390 Ω, 5%, ¼ W	101592
R10,25	Resistor, 1 k, 5%, ¼ W	101569
R11	Resistor, 2.7 k, 5%, ¼ W	101599
R12,14,23,32	Resistor, 4.7 k, 5%, ¼ W	101598

PARTS LIST

TIME BASE SERIAL PRESET/RESET #021566-7-11 (Cont'd)

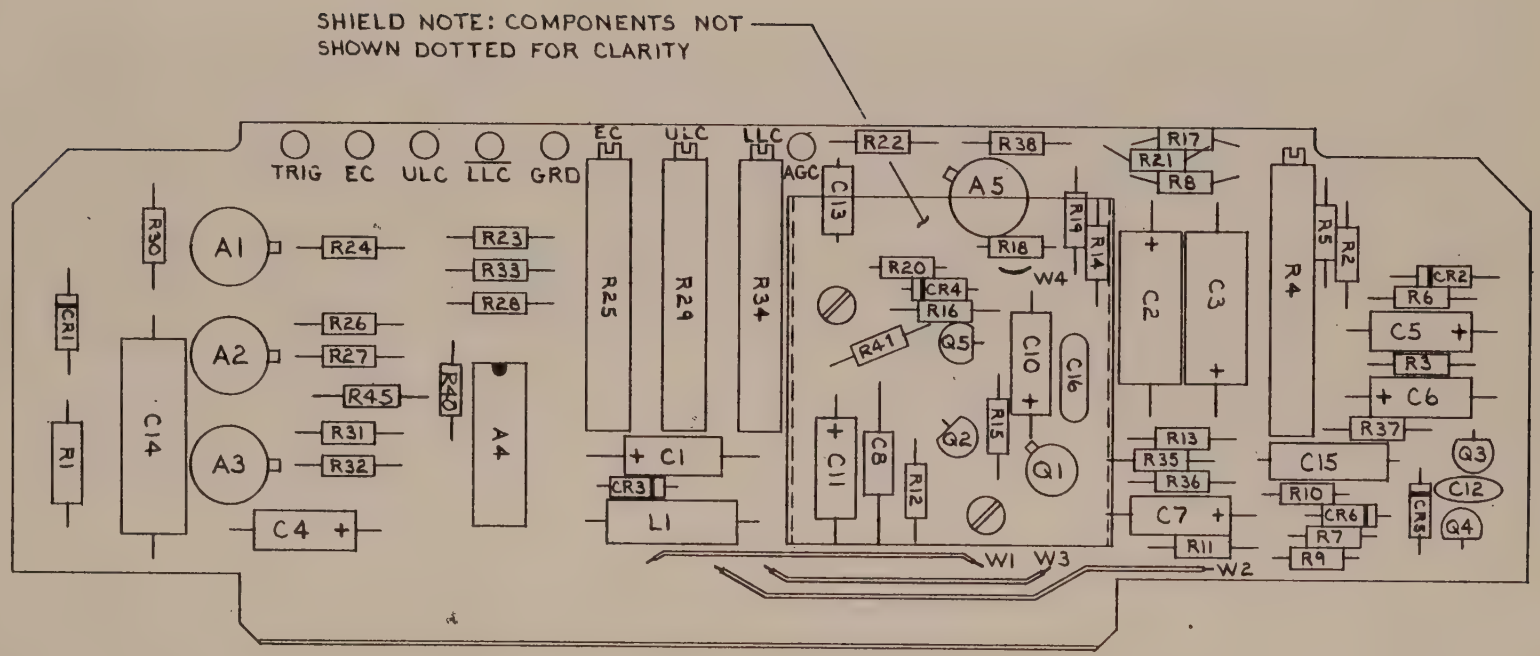
REF.	DESCRIPTION	SD PART NO.
R13,19-21,26, 28-30	Resistor, 10 k, 5%, ¼ W	101570
R16,18,27	Resistor, 8.2 k, 5%, ¼ W	101595
R22,31	Resistor, 470 Ω, 5%, ¼ W	101625
XY1	Crystal, Socket	100769
Y1	Crystal, 1 MHz	102450
	Extractor	100865



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. A1, A2, A3 ARE CA-3002
   A4 IS SN74132N
   A5 IS MC-14396
3. PIN 14 OF A4 IS CONNECTED TO Vcc
   " 7 " " " " " GRD.
4. R17, R21 ——— FACTORY SELECTED.

AGC & CYCLE DETECTOR SCHEMATIC #021569-7-1 REV S



AGC & CYCLE DETECTOR ASSEMBLY #021569-4-1 REV N

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-1 REV U

REF.	DESCRIPTION	SD PART NO.
	Assembly	021569-4-1
	Schematic	021569-7-1
A1-3	Integrated Circuit, CA3002	025701
A4	Integrated Circuit, SN74132N	045270
A5	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 47 µF, 20 V	100186
C4,10	Capacitor, 22 µF, 15 V	100125
C5	Capacitor, 4.7 µF, 35 V	100071
C6,11	Capacitor, 10 µF, 20 V	100063
C7	Capacitor, 2.2 µF, 35 V	100100
C8	Capacitor, .1 µF, 100 V	100141
C12	Capacitor, .001 µF	100076
C13	Capacitor, .0022 µF	100185
C14	Capacitor, 20 µF, 25 V	100264
C15	Capacitor, .01 µF, 200 V	100168
C16	Capacitor, 470 pF	100283
CR1	Diode, 1N748A	100384
CR2	Diode, 1N961B	100395
CR3-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1	Transistor, 2N5363	101403
Q2	Transistor, 2N5459	101384
Q3-5	Transistor, 2N3906	101378
R1	Resistor, 330 Ω 5%, 1/2 W	101474
R2	Resistor, 10 M 5%, 1/4 W	101564
R3	Resistor, 12 k 5%, 1/4 W	101565
R4,34	Potentiometer, 5 k Beckman 78P, Var	101938
R5	Resistor, 2.7 k 5%, 1/4 W	101599
R6,41	Resistor, 100 k 5%, 1/4 W	101558
R7	Resistor, 4.7 k 5%, 1/4 W	101598
R8	Resistor, 820 Ω 5%, 1/4 W	101567
R9	Resistor, 100 Ω 5%, 1/4 W	101609
R10	Resistor, 39 k 5%, 1/4 W	101561
R11	Resistor, 47 k 5%, 1/4 W	101574
R12,13,20	Resistor, 270 k 5%, 1/4 W	101769
R14	Resistor, 220 Ω 5%, 1/4 W	101566
R15	Resistor, 1.2 k 5%, 1/4 W	101581
R16,18,30	Resistor, 2.2 k 5%, 1/4 W	101562

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-1 (Cont'd)

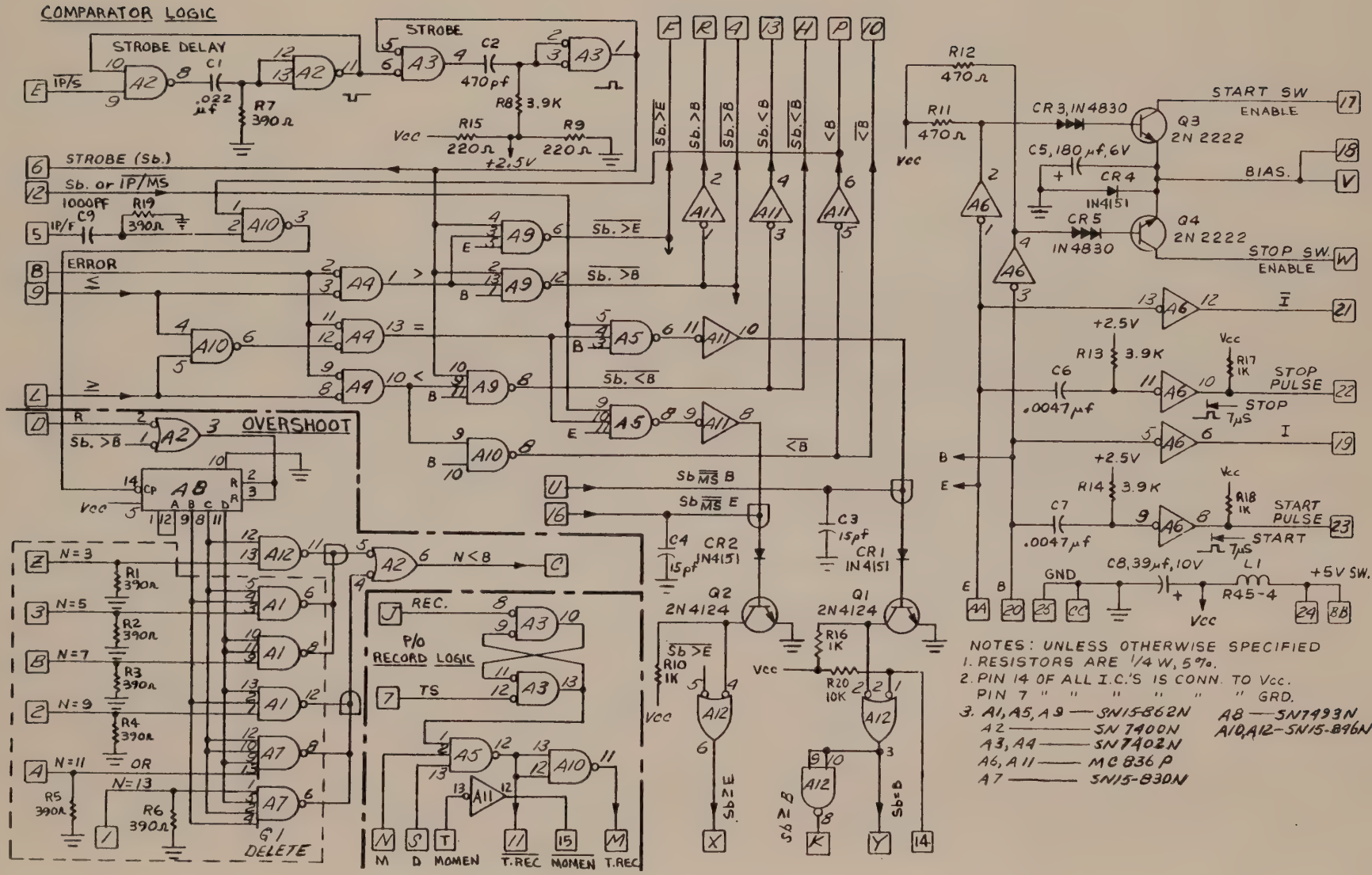
REF.	DESCRIPTION	SD PART NO.
R19	Resistor, 4.7 Ω 5%, 1/4 W	101796
R23,38	Resistor, 10 k 5%, 1/4 W	101570
R23,40,45	Resistor, 1 k 5%, 1/4 W	101569
R24	Resistor, 5.6 k 5%, 1/4 W	101584
R25	Potentiometer, 10 k Beckman 78P	101918
R26	Resistor, 15 k 5%, 1/4 W	101552
R27,32	Resistor, 3 k 5%, 1/4 W	101548
R28,33	Resistor, 470 Ω 5%, 1/4 W	101625
R29	Potentiometer, 2 k Beckman 78P	101876
R31	Resistor, 3.3 k 5%, 1/4 W	101559
R35,36	Resistor, 47 Ω 5%, 1/4 W	101560
R37	Resistor, 27 k 5%, 1/4 W	101587
W1-4	Wire, #24 AWG solid bus	
	Shield, AGC	021421-1-1
	Spacer	100934
	Insulator	021427-1-1
	Extractor	100865

CIRCUIT DESCRIPTION
COMPARATOR LOGIC
SCHEMATIC #021583-7-1

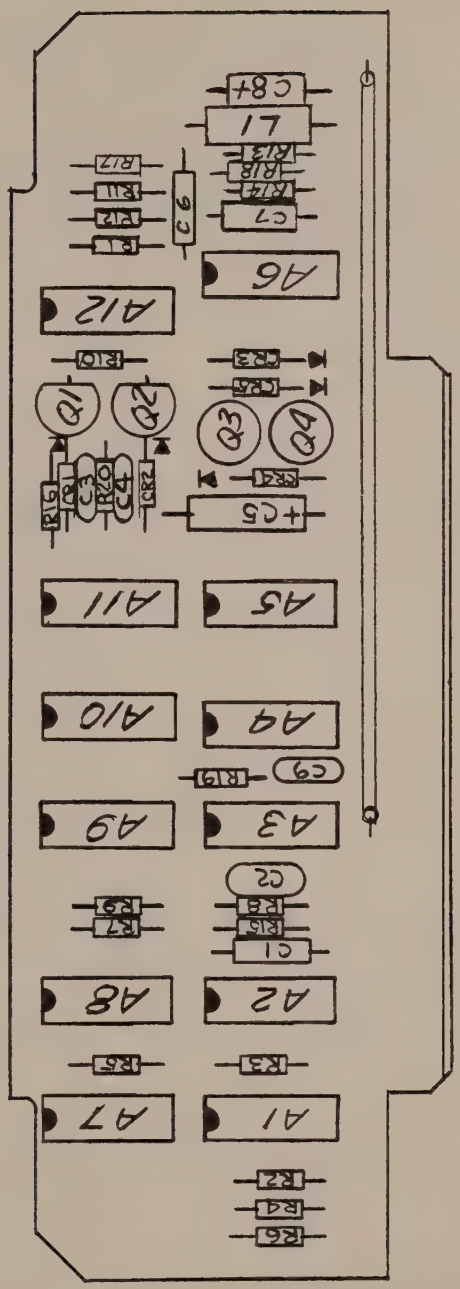
1) GENERAL

The Comparator Logic Card is one of a group of three cards which contain the comparator and control logic circuitry. The other two are the Mode Logic Card A24 and the Function Logic Card A25. The functional description of the circuitry on these cards is provided in Chapter 5.

The Comparator Logic Card contains the bulk of the comparator logic circuitry plus the Overshoot Logic.



COMPARATOR LOGIC SCHEMATIC #021583-7-1B



COMPARATOR LOGIC ASSEMBLY #021583-4-1A

PARTS LIST

COMPARATOR LOGIC #021583-7-1

REF.	DESCRIPTION	SD PART NO.
	Assembly, Comparator Logic	021583-4-1
	Schematic, Comparator Logic	021583-7-1
A2	Integrated Circuit, SN7400N	019705
A3,4	Integrated Circuit, SN7402N	025709
A5,9	Integrated Circuit, SN15-862N	019719
A6,11	Integrated Circuit, MC836P	025704
A8	Integrated Circuit, SN7493N	025715
A10,12	Integrated Circuit, SN15-846N	019716
C1	Capacitor, .022 µF, 200 V, Mylar	100130
C2	Capacitor, 470 pF, DM15	100221
C3,4	Capacitor, 15 pF, DM15	100241
C5	Capacitor, 180 µF, 6 V, Tant	100207
C6,7	Capacitor, .0047 µF, 200 V, Mylar	100129
C8	Capacitor, Elect., 39 µF, 10 V	100183
C9	Capacitor, 1000 pF, DM15	100243
CR1,2,4	Diode, 1N4151	100385
CR3,5	Diode, 1N4830	100440
L1	Inductor, Nat., R45-4	101313
Q1,2	Transistor, 2N3904	101377
Q3,4	Transistor, 2N2222	101347
R7,19	Resistor, 390 Ω, 1/4 W, 5%, CC	101592
R8,13,14	Resistor, 3.9 k, 1/4 W, 5%, CC	101601
R9,15	Resistor, 220 Ω, 1/4 W, 5%, CC	101566
R10,16-18	Resistor, 1 k, 1/4 W, 5%, CC	101569
R11,12	Resistor, 470 Ω, 1/4 W, 5%, CC	101625
R20	Resistor, 10 k, 1/4 W, 5%, CC	101570
	Extractors	100865

CIRCUIT DESCRIPTION
READER LOGIC
SCHEMATIC #021588-7-3

1) GENERAL

Signals, $\overline{LLC}$ and EC respectively, are connected to pins A and 1 of the Reader Logic Card. The Reader Logic circuit accepts the EC and $\overline{LLC}$ signals and detects the ONES, ZEROS and MARKS in the code. These signals are used to shift the BCD time information of the input code into a shift register and then transfer it to the Time of Day Accumulator Card which drives the Display drivers and Code Generator.

2) FUNCTIONAL

The basic scheme is as follows:

When a MARK is detected, the 9-bit shift-register (A14) and 1/2 (A13) is cleared and a ONE set in the first bit position. Also, the "Y" counter (A10) is advanced one.

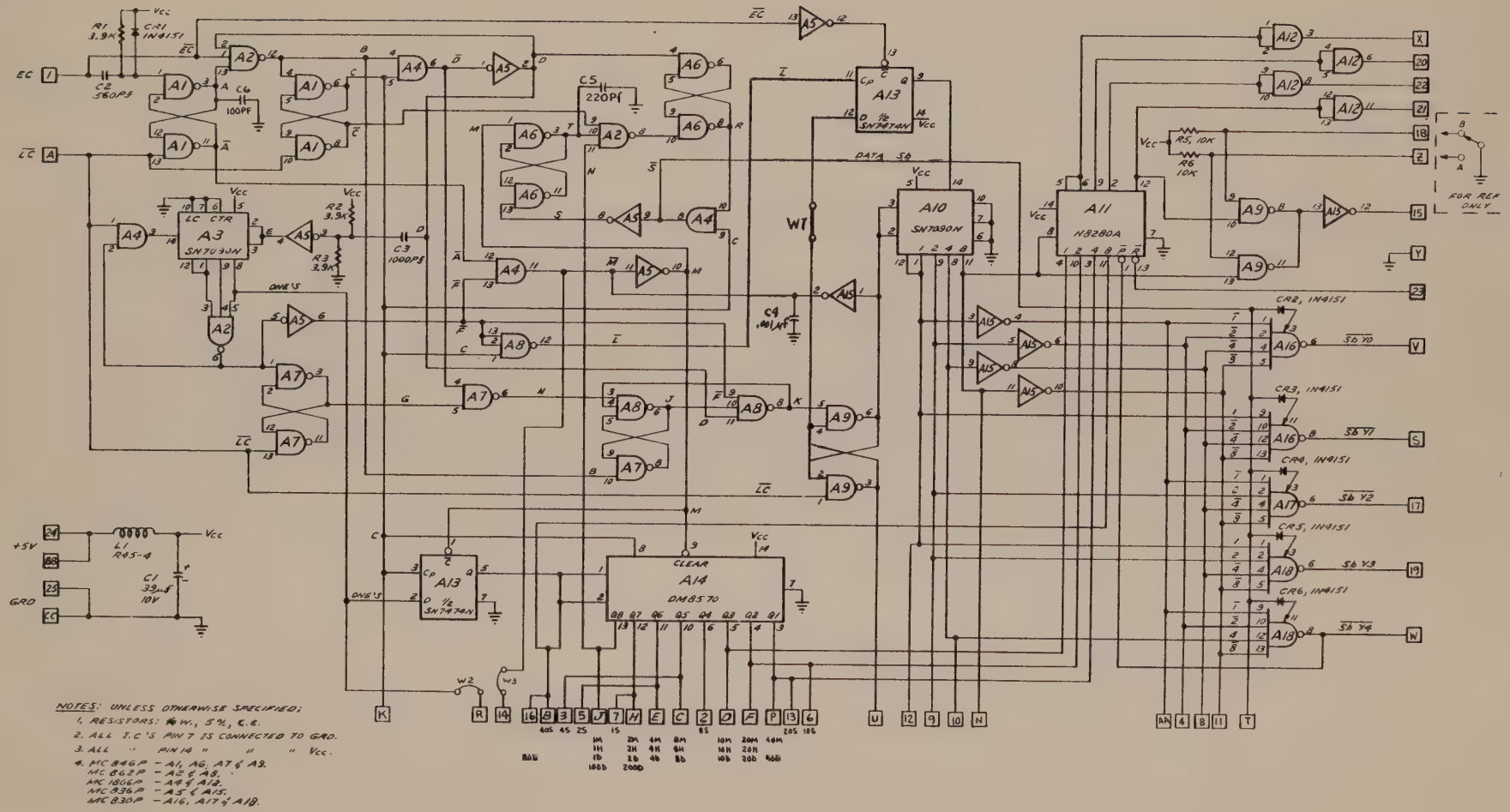
When the second MARK of the double MARK is detected, the sequence is changed so that the "Y" counter is set to ZERO if it was not already at ZERO. The "Y" counter is not advanced for this MARK, nor is the shift register cleared. However, the ONE that was entered by the first MARK is shifted one position. The shift register is now advanced one position for each binary bit of the time frame. When the ONE that was entered by the first MARK reaches the ninth position, a circuit is set which permits the next shift signal to transfer the information from the register to the seconds section of the Time of Day Accumulator.

When the MARK is detected, the register is cleared, a ONE entered, and the "Y" counter advanced one. After 9-bits are shifted into the register, the information is transferred to the minutes section of the Time of Day Accumulator. This cycle of operation is repeated a third time for hours information. If Days Option, E20, is included, two additional cycles transfer this information to the Days Accumulator. The "Y" counter continues to count MARKS throughout the time frame.

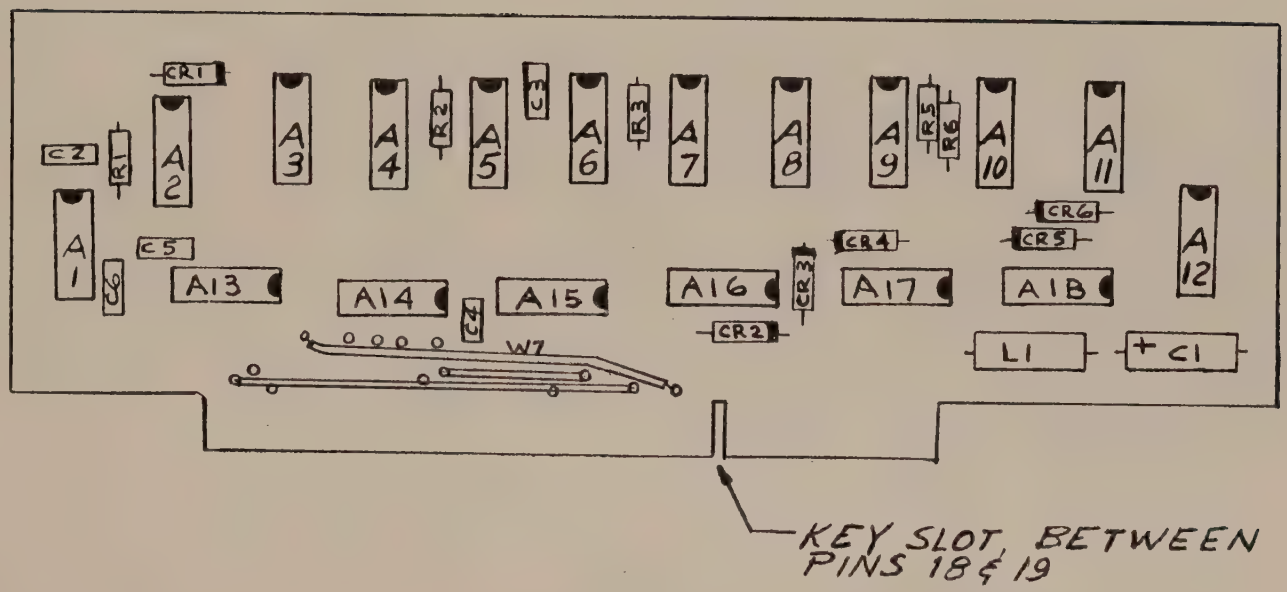
When the first MARK of the next double MARK is detected, it steps the "Y" counter from 9 to zero, advancing the Time of Day Accumulator one second. It is thus, updated at the beginning of the frame, and will contain the same information (assuming no errors) scanned-in during the frame.

The readout does not change during scan-in since the Time of Day Accumulator is already updated.

The serial level shift code at pin R is fed to the Error Bypass circuit where it is compared with the output from the Code Generator which represents, in serial form, the contents of the Time Accumulator.



READER LOGIC SCHEMATIC #021588-7-3 REV D



READER LOGIC ASSEMBLY #021588-4-3 REV B

PARTS LIST

READER LOGIC #021588-7-3

REF.	DESCRIPTION	SD PART NO.
	Assembly, Reader Logic	021588-4-3
	Schematic, Reader Logic	021588-7-3
A1,6,7,9	Integrated Circuit, MC846P	019716
A2,8	Integrated Circuit, MC862P	019719
A3,10	Integrated Circuit, SN7490N	025732
A4,12	Integrated Circuit, MC1806P	025733
A5,15	Integrated Circuit, MC836P	025704
A11	Integrated Circuit, N8280A	025722
A13	Integrated Circuit, SN7474N	025241
A14	Integrated Circuit, DM8570	025751
A16,17,18	Integrated Circuit, MC830P	019712
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF, Mica	100222
C3	Capacitor, .001 µF, DM15	100243
C4	Capacitor, .001 µF, Disc	100076
C5	Capacitor, 220 pF, DM15	100220
C6	Capacitor, 100 pF	100173
CR1-6	Diode, 1N4151	100385
L1	Inductor	101313
R1-3	Resistor, 3.9 k, 1/4 W, 5%, CC	101601
R5,6	Resistor, 10 k, 1/4 W, 5%, CC	101570
W2,3,7	Wire, Insulated, 24GA	
	Extractor	100865

CIRCUIT DESCRIPTION
FWD/REV CONTROL
SCHEMATIC #021625-7-1

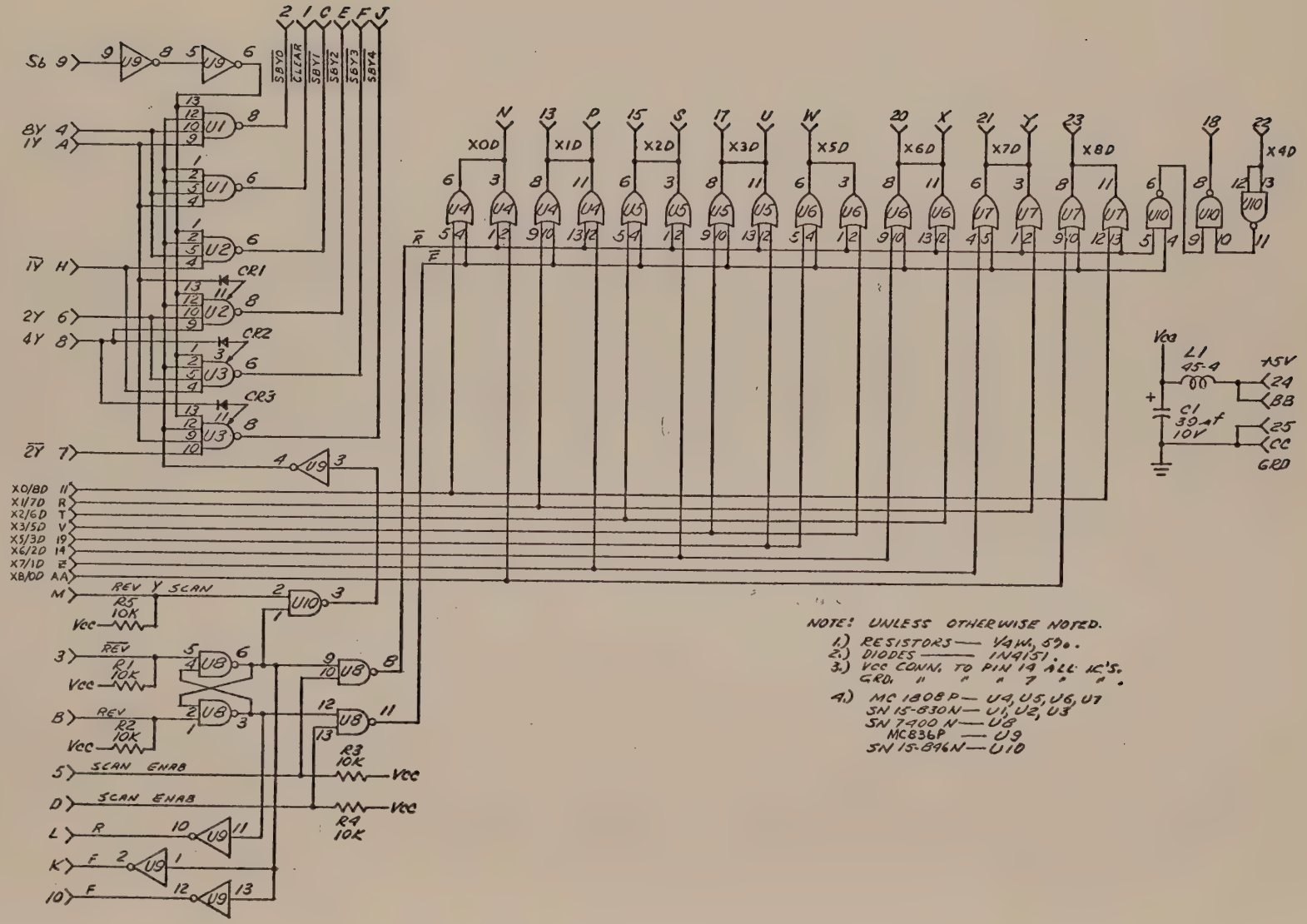
1) GENERAL

The FWD/REV Control card (A13) contains gates which invert the order of the time data bits stripped from the input code when reading a reverse code. In addition, it provides buffered forward and reverse control signals and establishes the Y Strobe signals needed to load data into the Time Accumulator when operating with a reverse code. This circuitry is active only when operating in one of the search modes. All circuits are disabled in the PRESET and GENERATE modes.

2) OPERATION

Referring to Dwg #21625-7-1, the FWD and REV signals from the Tape Search section are fed to pins 3 and B, respectively. When operating in reverse (tape transport moving in a reverse direction) the FWD ($\overline{REV}$) signal is at ground, and the REV signal is positive. Flip-flop U8-6/3 is set. The positive output from U8-6 is fed to four circuits: 1) through U10-3 and U9-4, opening Y Strobe Scan gates U1, U2, and U3; 2) through U8-8, opening gates U4-3, U4-11, U5-3, U5-11, U6-3, U6-11, U7-3, and U7-11 to negative time data signals $\overline{X0}$ through $\overline{X8}$; 3) through U9-2 to the Error Bypass circuit, disabling forward Y Scan; and 4) through U9-12, clamping the Z-Rate signal at ground, thus blocking update of the TOD Accumulator (A15) and inhibiting operation of the Code Generator (A17) and Modulator (A8) circuits. The Y Strobe Scan gates load the rearranged data bits into the TOD Accumulator (A15) as each frame is stripped from the input code.

When forward operation is established, flip-flop U8-6/3 is reset. The Y Strobe Scan gates are disabled (all outputs driven positive), gates U4-6, U4-8, R5-6, U5-8, U6-6, U6-8, U7-6, and U7-8 are open (time data restored to normal order); U9-12 and U9-2 outputs are up, restoring normal operation of the TOD Accumulator, Code Generator, Modulator, and Error Bypass circuitry.



FWD/REV CONTROL SCHEMATIC #021625-7-1

FWD/REV CONTROL ASSEMBLY #021625-4-1 REV A

PARTS LIST
FWD/REV CONTROL #021625-7-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021625-4-1
	Schematic	021625-7-1
C1	Capacitor, 39 µF, 10 V	100183
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1-5	Resistor, 10 k, 1/4 W, 5%	101570
U1-3	Integrated Circuit, SN15-830N	019712
U4-7	Integrated Circuit, MC1808P	025734
U8	Integrated Circuit, SN7400N	019705
U9	Integrated Circuit, MC836P	025704
U10	Integrated Circuit, SN15-846N	019716
	Extractor	100865

CIRCUIT DESCRIPTION
MINOR COUNTER
SCHEMATIC #021632-7-2

1) GENERAL

The Minor Counter card (A9) can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. Provision is included for three output pulse rates with 10% duty cycle which may be supplied in place of the days recycle circuit.

2) DECADE DIVIDERS

The up to three decade dividers (A1, A4, A6) are connected in tandem. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. Jumpers W1 and W2 permit the data strobe associated with the center decade (A4) to be wired in common with the data strobe input to the first decade (A1) or the third (A6). The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the two sets (A10, A13 and A15) can be gated by inputs through pins L, K and J, respectively. These gate lines are buffered by inverters on A11.

4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

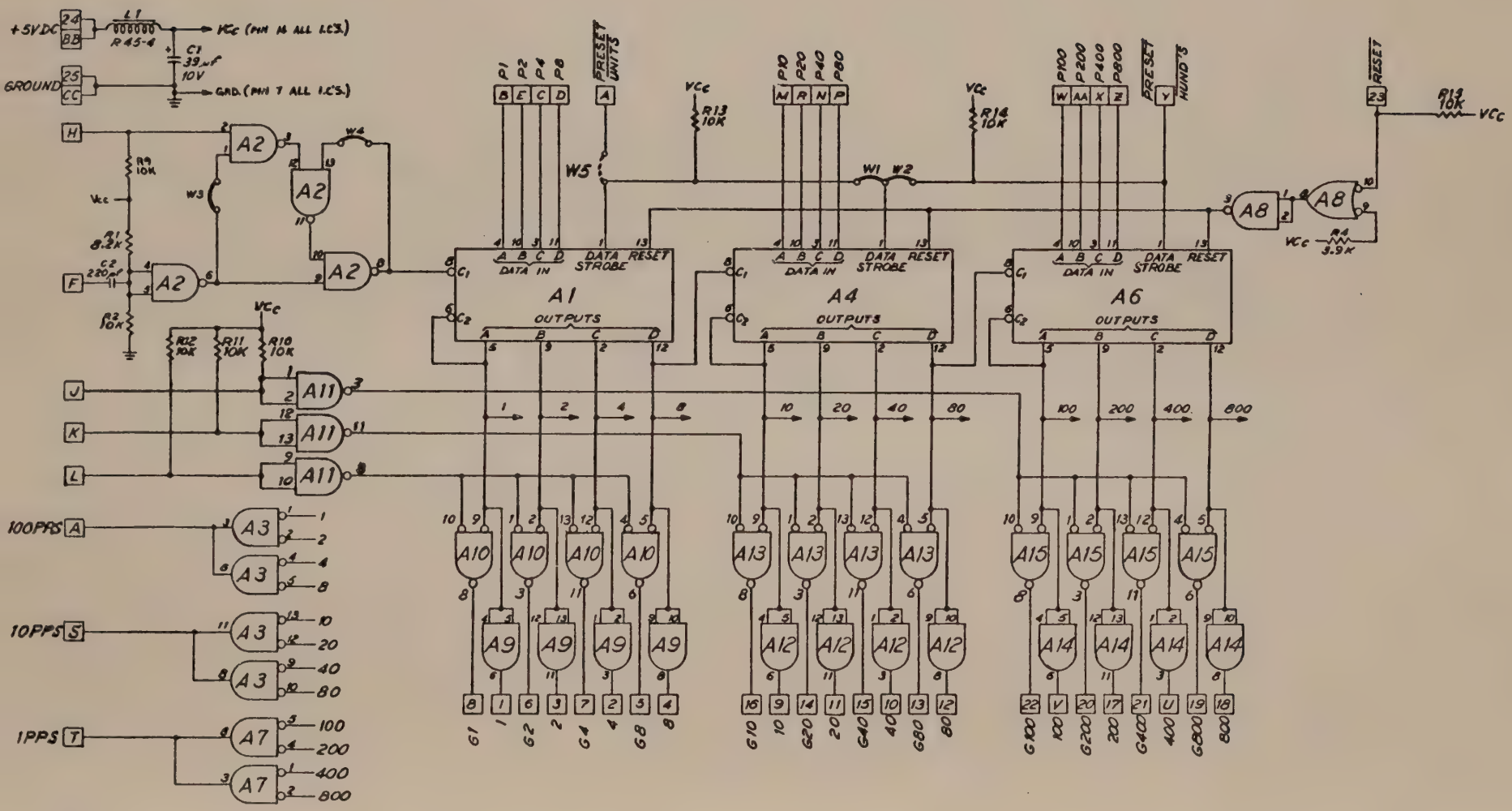
A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8/11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) OUTPUT PULSE RATES

Three sets of gates are used to produce three 10%-duty-cycle pulse rates. Each pulse goes high when the four outputs from the corresponding decades are low (leading edge on time). The pulse remains up until the output of the decade is 001. Thus, the pulse is high 10% of the time. The output is a 5 V logic level behind 6 kΩ.

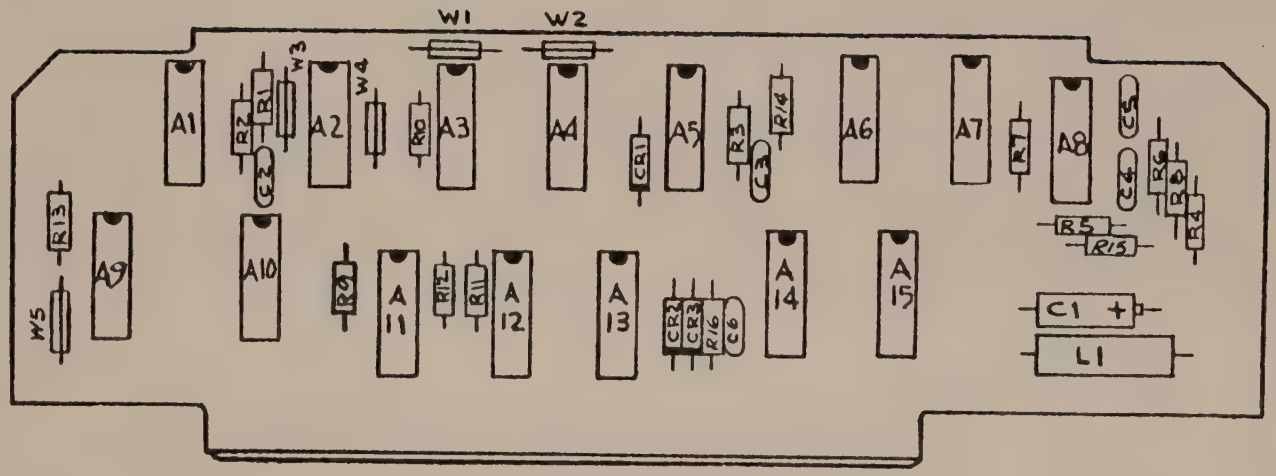
The pulse rate outputs are fed to pins A, S and T which are used for units preset and days recycle inputs on other configurations of the card. Chip A5 (see assembly #021632-4-1) is removed when the rate outputs are supplied.

8154-2-79



MINOR COUNTER SCHEMATIC #021632-7-2 REV B

5-82



MINOR COUNTER ASSEMBLY #021632-4-1 REV C

PARTS LIST

MINOR COUNTER #021632-7-2

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #021632-4-1)	021632-4-2
	Schematic	021632-7-2
A1,4,6	Integrated Circuit, N8280A	025722
A2,11	Integrated Circuit, MC846P	019716
A3,7	Integrated Circuit, MC1810P	025735
A8	Integrated Circuit, SN7400N	019705
A9,12,14	Integrated Circuit, MC1806P	025733
A10,13,15	Integrated Circuit, MC1808P	025734
C1	Capacitor, 39 µF, 10 V, Tant	100183
C2	Capacitor, 220 pF, 500 V, +10%, DM	100220
L1	Inductor, R45-4	101313
R1	Resistor, 8.2 k, 5%, 1/4 W, CC	101595
R2,9-15	Resistor, 10 k, 5%, 1/4 W, CC	101570
R4	Resistor, 3.9 k, 5%, 1/4 W, CC	101601
W1-4	Jumper, Molded	102879

CIRCUIT DESCRIPTION
PRESET AND ERROR BYPASS
SCHEMATIC #7-05153802

1) GENERAL

This card contains Preset Control, Error Bypass, Pulse Rate, Z-Rate, FWD/REV, and Reset circuits. It is used in the Model 8132 Reader, the Model 8134 Reader/Search Unit, the Model 8152 Generator/Reader and the Model 8154 Generator/Reader/Search Unit.

2) OPERATION

PRESET CONTROL: Referring to the lower right corner of the schematic, Preset Logic is provided for detecting TOD and Days Coincidence in the Model 8154 Time Code Generator/Reader/Search Unit. When armed in the PRESET Mode, these circuits combined with the comparator, detect coincidence between the time entered on the front panel PRESET/START TIME thumbwheel switches and the contents of the accumulator. The coincidence signals are sent to preset control circuits on Time Base & Control Card A27. When Days/ID Option E13 is included, these circuits separate the Days and TOD sections of the comparator providing separate Days and TOD Coincidence outputs to Card A27.

ERROR BYPASS: The Error Bypass circuit is shown at the top of the schematic. It is enabled in the READ Forward Mode of Operation only and includes provision for selecting 0, 3, 5, 7, or 9 frames of Error Bypass. This means that data stripped from the input code will not be loaded into the Accumulator until after the selected number of consecutive error frames has been counted. (READ Reverse is equivalent to "0" error bypass in which all data are loaded into the Accumulator irrespective of errors.)

The Error Bypass circuit accepts the serial level shift output from the Reader Logic Card and compares it with the serial level shift output from the Code Generator Card in exclusive OR gate U13-11. The output from this gate is fed to gate U7-6 along with blanking and sampling signals which differ as a function of the code being read and the options present in the Reader.

The sampling signal from U14-2 is developed in Counter/Decoder U1/U2 from the Z-Rate input and selected by U3. It is a pulse at Z4 time for IRIG and NASA Codes and at Z5 time for XR3 Code.

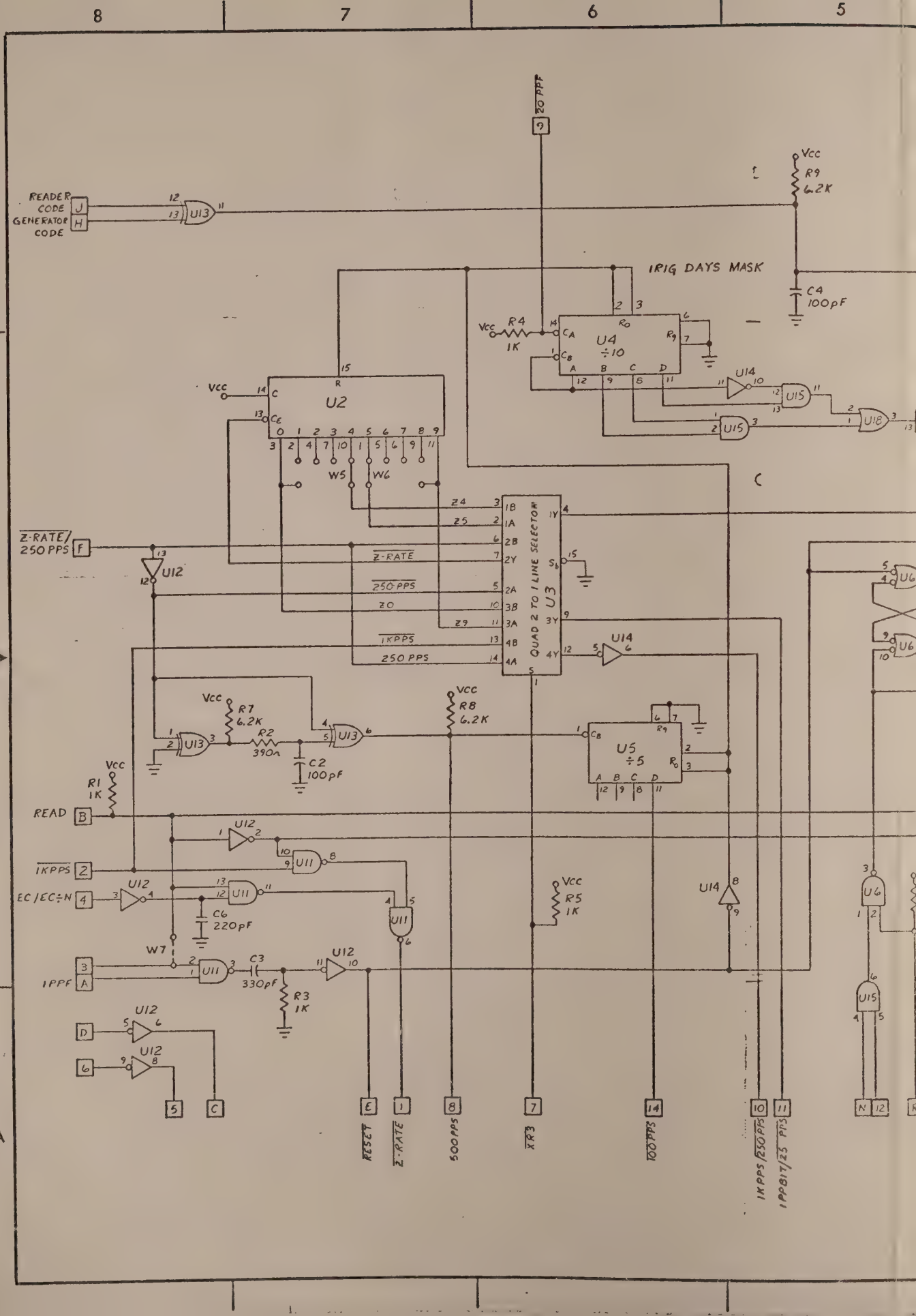
The IRIG Days Mask from U14-12 is developed by Counter U4 and associated decoding gates from the 20 ppF input to pin 9. It inhibits comparison of days bits so that readers without the Days Option can read IRIG Codes containing days.

The blanking signal from flip-flop U6-6, 8 restricts comparison to that portion of the code containing time information. It is set by the differentiated leading edge of the 1 ppF input through U11-3, C3, U12-10

($\overline{\text{RESET}}$), and cleared by the output from the 3 input NAND gate formed from U15-6 and U6-3. The $\overline{\text{RESET}}$ signal clears flip-flop U10-3/U6-11 provided it was set by the detection of at least one error (U7-6 output going low) during the previous frame. Assuming that no error has occured, this flip-flop will not be set and output U6-11 will be high opening gate U10-6. When the clear signal from U6-3 occures during the current frame, it is inverted by U19-2 and fed through U10-6 resetting counter U9 and flip-flop U7-8/U10-8. The low output from U7-8 is fed through U20-3 and U20-8 to pin 23 and the Reader Logic Card, inhibiting forward Y-Scan. (Gates U20-3, 8 are open in READ Forward only.) This same signal is fed through U20-11 to pin 20. The resulting output is used to enable the comparators in tape search units. Now, if an error occurs during the next frame, flip-flop U10-3/U6-11 will be set (with U10-3 high and U6-11 low) and, when U6-3 output goes low during the frame, U10-6 will be closed and counter U9 will not be reset. The $\overline{\text{RESET}}$ signal at the start of the next frame clears flip-flop U10-3/U6-11 and counter U9 accumulates one count. If the next frame is good, U9 is reset and the count starts over. If the next frame is bad, however, U9 accumulates a second count. The BCD outputs from counter U9 are decoded by U8 and fed to a set input to flip-flop U7-8/U10-8 through gates on U17 which are used to select the desired number of error bypass frames. When counter U9 reaches this number, flip-flop U7-8/U10-8 is set enabling forward scan of the time data (stripped from the input code by the Reader Logic during the next frame) into the Accumulator. The tape search comparators, when present, are inhibited by the output from U20-11 during this one frame. Counter U9 is reset through U19-4 and U10-11 and the sequence starts again. The selected number of consecutive error frames must occur before the input time data is permitted to be loaded into the Accumulator.

PULSE RATES: Selected pulse rates from U3 through U14-4 and U14-6 and from edge detector U13-3, 6 and counter U5 are provided as outputs when XR3 Time Codes are being read.

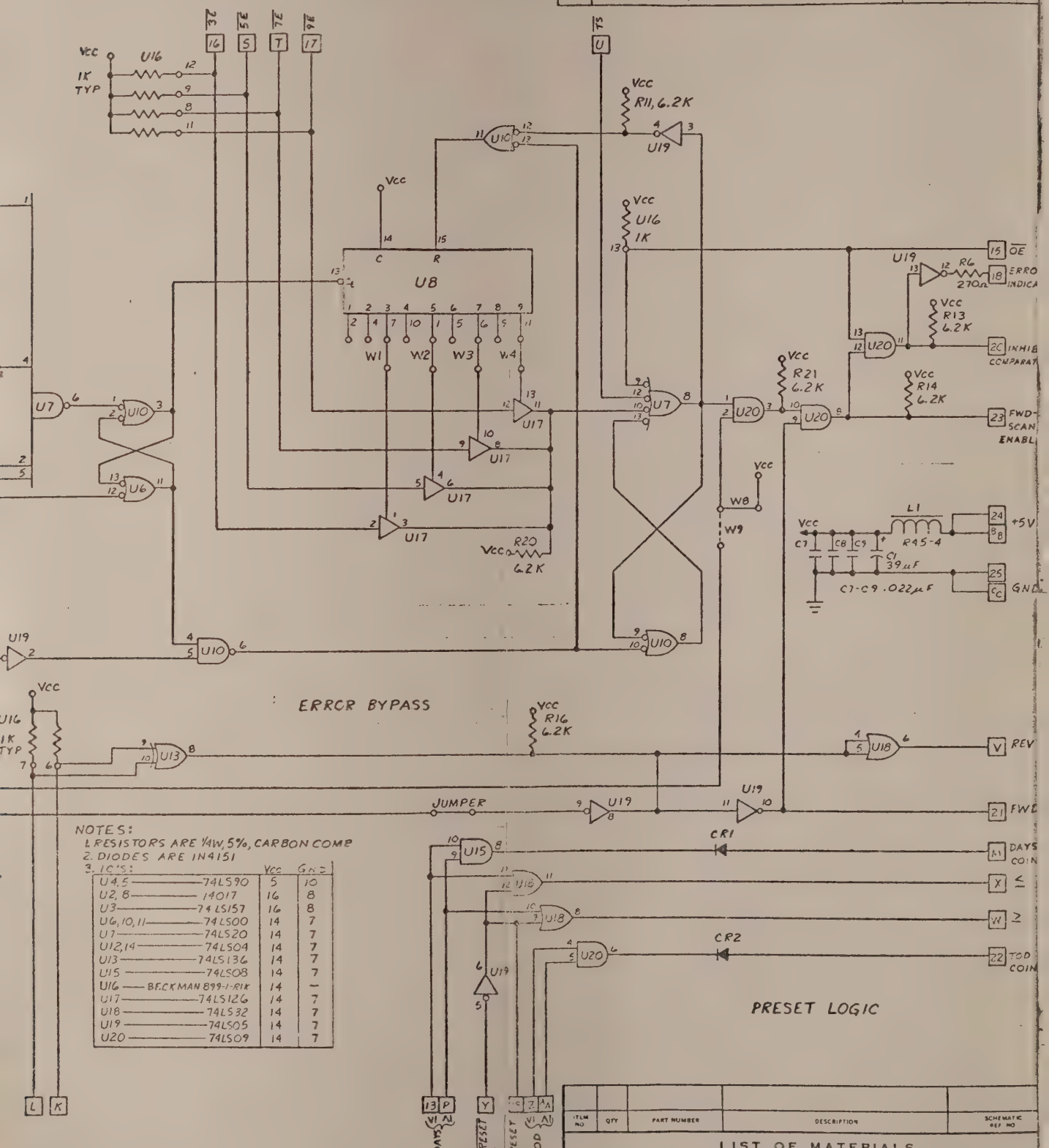
Z-RATE and RESET: These circuits, shown at the lower left on the schematic, select Z-Rate output for GENERATE and READ and develope a $\overline{\text{RESET}}$ pulse from the leading edge of the 1 ppF input.


8
7
6
5
D
C
B
A
READER CODE GENERATOR CODE
U
H
U13
20 PPF
9
Vcc
R9
6.2K
C4
100pF
IRIG DAYS MASK
Vcc
R4
1K
U4
÷10
U14
U15
U18
U2
W5
W6
Z4
Z5
Z-RATE
250 PPS
Z0
Z9
1KPPS
250 PPS
U3
QUAD 2 TO 1 LINE SELECTOR
Z-RATE/
250 PPS
F
U12
R7
6.2K
R2
390Ω
C2
100pF
R8
6.2K
U5
÷5
R1
1K
READ
B
1KPPS
2
EC/EC÷N
4
C6
220pF
W7
1PPF
3
A
C3
330pF
R3
1K
R5
1K
D
6
5
C
E
1
8
7
14
10
11
RESET
Z-RATE
500PPS
XR3
100PPS
1K PPS/250 PPS
1 PPBIT/25 PPS
N
12

B	CHG'D IC'S, R3,6,C3; ADD'D R7-16.	17167	
C	REDESIGNED W/OUT U1 & U9.	17515	

REVISIONS

REV	DESCRIPTION	SHT NO	BLD NO	DATE	APP
A					
A1	DELETED W9; ADD'D W8. (ECP 019-79)		NFC		



NOTES:
1. RESISTORS ARE 1/4W, 5%, CARBON COMP
2. DIODES ARE 1N4151
3. IC'S:

		Vcc	GND
U4,5	74LS90	5	10
U2, 8	14017	16	8
U3	74LS157	16	8
U6,10,11	74LS00	14	7
U7	74LS20	14	7
U12,14	74LS04	14	7
U13	74LS136	14	7
U15	74LS08	14	7
U16	BECKMAN 899-1-R1K	14	—
U17	74LS126	14	7
U18	74LS32	14	7
U19	74LS05	14	7
U20	74LS09	14	7

ITEM NO	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

PROPRIETARY DATA

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8154	
8152	
8134	
8122	
USED ON	NEXT ASSY
APPLICATION	

DRAWN 5-8-81 CHECK DATE ELECT. DATE MECH. DATE PROJECT DATE QA DATE SCALE Ø DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE X .XX .XXX ANGLES ±

SH 1 OF 1

BYSTRON DONNER CORPORATION CONCORD, CALIFORNIA

CODE IDENT. 52542

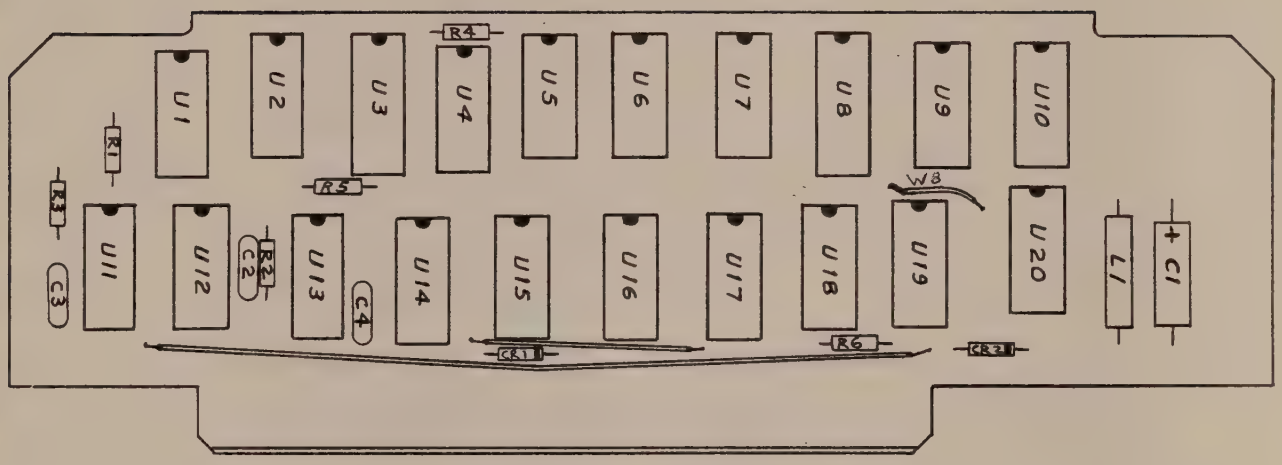
MATERIAL

PRESET AND ERROR BYPAS

DRAWING NO

REF	SIZE	PART NO.
	D	05153802

5-87



PRESET/ERROR BYPASS ASSEMBLY #05153802 REV A_1

PARTS LIST

PRESET & ERROR BYPASS #05153802 REV A_2

REF.	DESCRIPTION	SD PART NO.
	Assembly	05153802
	Schematic	7-05153802
C1	Capacitor, 39 µF, 10 V	100183
C2,4	Capacitor, 100 pF	100173
C3	Capacitor, 1000 pF	100243
CR1,2	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1,4,5	Resistor, 1 k, 5%, ¼ W	101569
R2,3	Resistor, 390 Ω, 5%, ¼ W	101592
R6	Resistor, 270 Ω, 5%, ¼ W	101542
U1,4,5,9	Integrated Circuit, SN7490N	025732
U2,8	Integrated Circuit, SN7442N	025749
U3	Integrated Circuit, SN74157N	045242
U6,10,11	Integrated Circuit, SN7400N	019705
U7	Integrated Circuit, SN7420N	025713
U12,14	Integrated Circuit, SN7404N	025779
U13	Integrated Circuit, MC1812P	025736
U15,20	Integrated Circuit, MC1806P	025733
U16	Integrated Circuit, (Beckman 899-1-R1k)	116454
U17	Integrated Circuit, MC1808P	025734
U18	Integrated Circuit, SN7432N	045257
U19	Integrated Circuit, MC836P	025704
W8	Wire, Jumper	
	Extractor	100865

CIRCUIT DESCRIPTION
POWER SUPPLY
SCHEMATIC #041810-7-9

1) GENERAL

The power supply provides four regulated dc voltages (±5 V and ±15 V), five unregulated dc voltages (±9 V, ±21 V and +210 V), and an 18 V rms time base output at the line frequency. The regulated output voltage levels are adjustable. These outputs are current-limited and are short-circuit-proof to ground. (Note: Overheating may result if a short is maintained over an extended period of time.) Both voltage-sense and sense-return lines are provided for the regulated outputs. These lines are wired to provide regulation at the load. Fuses are provided for the unregulated +21 V and +210 V on the power supply assembly.

Input power is 115/230 V, 48 to 440 Hz at less than 100 watts with nominal line and all outputs fully loaded. (Note: The line frequency may be limited, 48 to 62 Hz unless option L12 is utilized, by the fan characteristics if a fan is included in the unit.) Input power is fed to transformer T1 through line filter Z1, fuse F1, a front panel power switch and 115/230 select switch, S101. The third wire is grounded to the chassis.

The transformer is constructed with split-primary windings which are connected in parallel for 115 V operation and in series for 230 V operation. Selection is made by 115/230 switch, S101. (Note: Units are normally shipped in the 115 V configuration with a 2A Slo-Blo fuse, F1. If the unit is converted to 230 V operation, F1 should be changed to 1A Slo-Blo.) Three secondary windings (two with center taps) are provided, one for ±9 V, one for ±21 V and 18 V rms, and the third for +210 V.

2) NONREGULATED SUPPLIES

The +210 V nonregulated supply is developed by the bridge rectifier formed from diodes CR5 through CR8, plus the filter circuit formed from R1, R2 and C5. The resulting output is fed through F2 (0.125A) to P103, pins 18 and V. It is used to drive front panel numerical indicating tubes and is rated at 100 mA.

The ±21 V nonregulated supplies are developed by bridge rectifier CR1 through CR4 and filtered by C1, C2, C8 and C11. The +21 V output is used internally as the source for the +15 V regulator. It is fed through F3 (1A) to P103, pins 15 and S, where it is available for use as a relay supply. The -21 V output is used internally as the source for the -15 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is also available at P103, pin 4, for external use. Each of the ±21V supplies is rated at 0.5A.

The 18 V rms is derived from the secondary winding which provides the ac voltage to develop the ±21 V. This rms voltage is fed through R15 to P103 pins 22 and Z.

The +9 V nonregulated supply is developed by full-wave rectifier CR11, CR12 and filtered by C3, C4 and C10. It is used internally as the source for the +5 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is available at P103, pins 21 and Y, for external use as a lamp supply. It is rated at 4A.

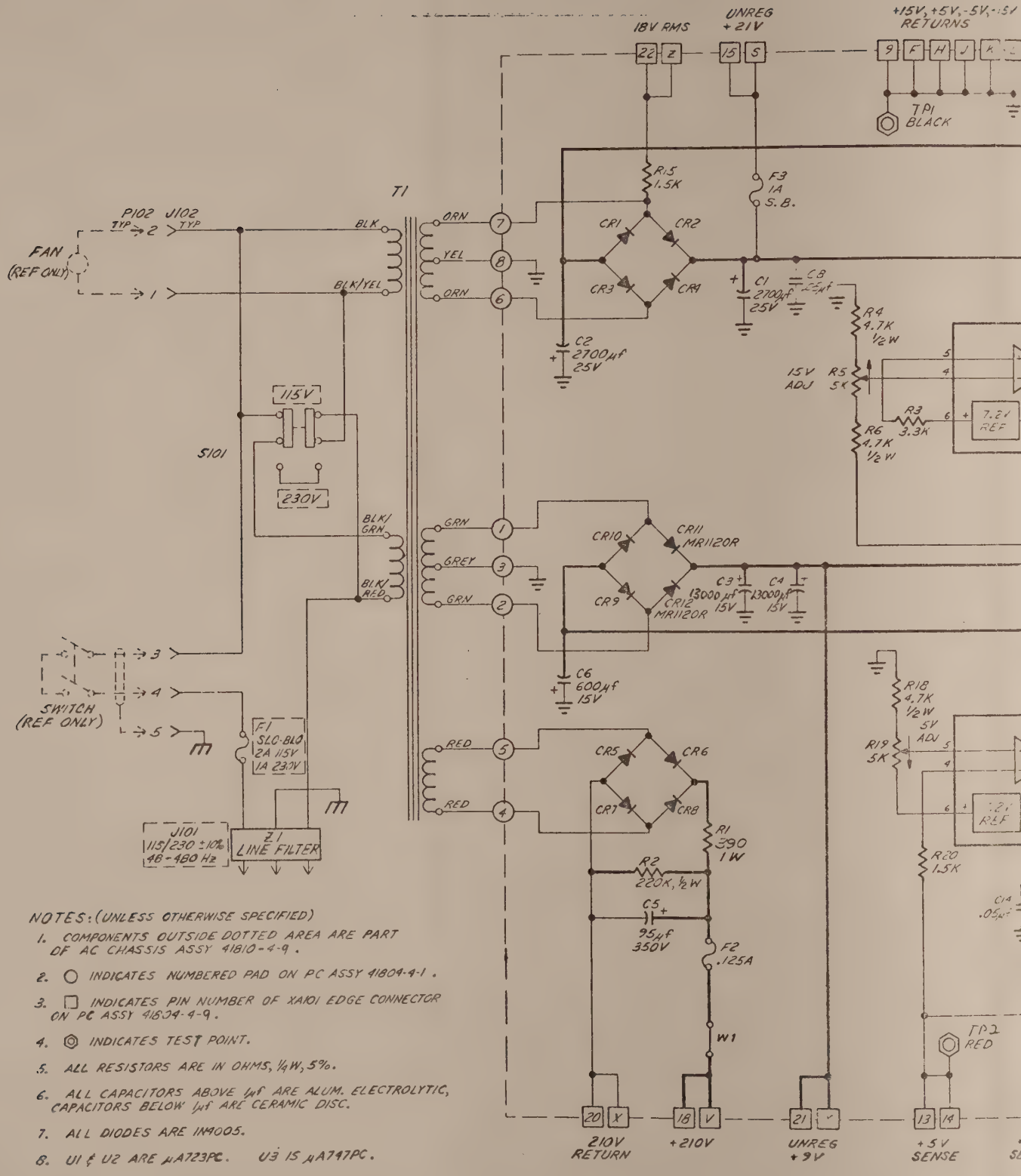
The -9 V nonregulated supply from full-wave rectifier CR9, CR10 and filter C6 is used internally as the source for the -5 V regulator. It is available at P103, pin 2, for external use. It is rated at 0.5A.

3) REGULATED SUPPLIES

The regulated +15 V, 0.5A output at P103, pin N, is established through pass transistor Q1 under the control of regulator U1 and the divider network (R4, R5, R6) between the +15 V SENSE line (P103, pin 12) and ground. The voltage on the arm of 15 V ADJ. potentiometer (R5) is fed to U1 where it is compared with the internal reference, referred to the ±15 V sense-return line (P103, pin 8). The current limit is imposed by sensing the drop across R9 and the circuit is stabilized by network R32, C7.

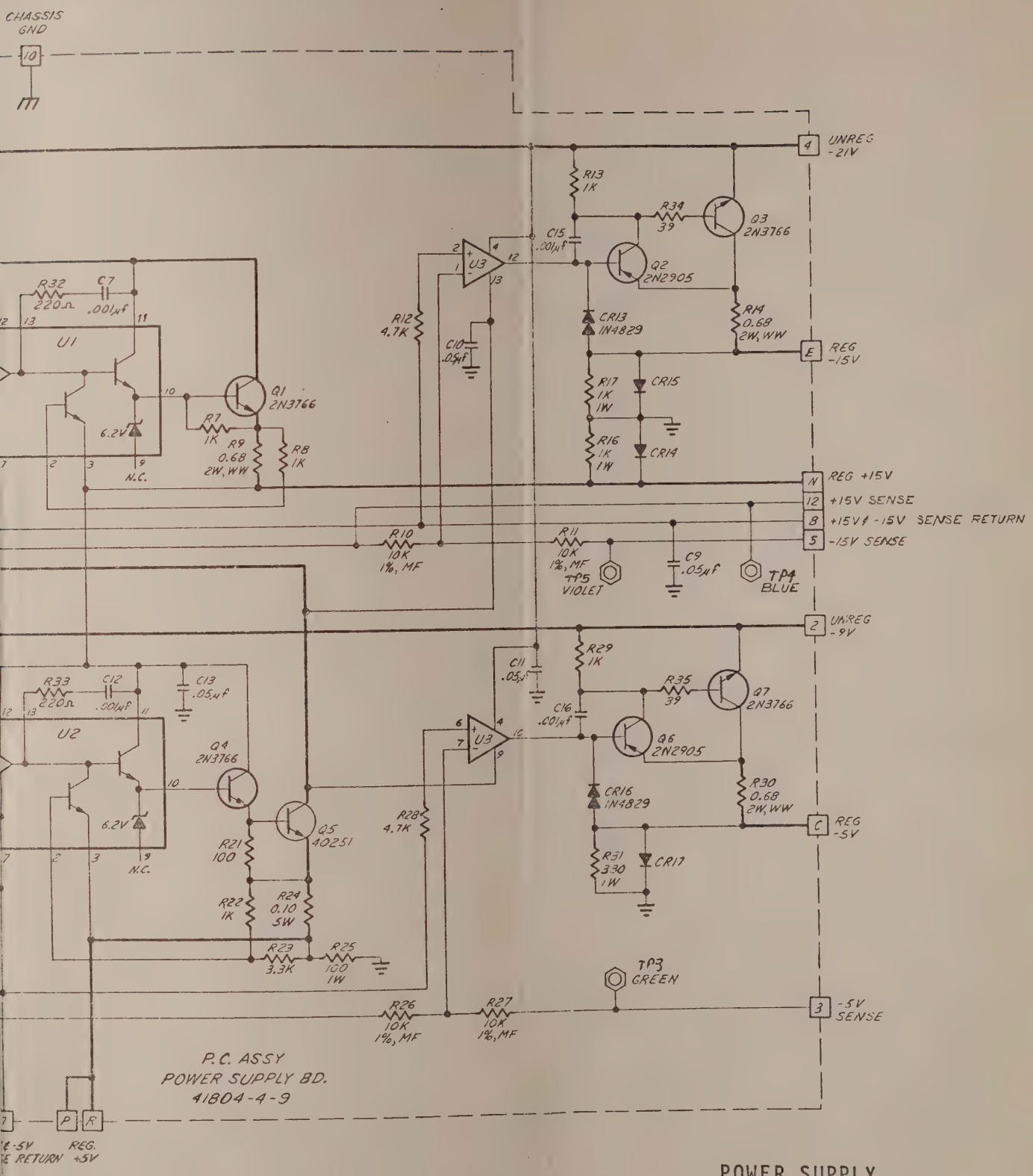
The regulated -15 V, 0.5A output at P103, pin 5, is established through Q2 and Q3 under the control of regulator amplifier U3-12. It uses the +15 V SENSE line as the reference, comparing it with the output through R10, R11 and the -15 V supply. Potentiometer R5 serves as the adjustment for both outputs. Current is limited by cutting the base drive to Q2 when the drop across R14 approaches one diode drop.

The regulated +5 V, 4A output at P103, pins P and R, is established through Q4 and Q5 under the control of regulator U2 and a divider network (R18, R19). The +5 V SENSE line at P103, pins 13 and 14, is compared with the fraction of the U2 internal reference voltage appearing on the arm of 5 V ADJ. potentiometer (R19). The current limit is imposed by sensing the drop across R24 through divider R22, R23. The circuit is stabilized by network R33, C12. The regulated -5 V, 0.5A output at P103, pin C, is established through Q6 and Q7 under the control of regulator amplifier U3-10. It uses the +5 V SENSE line as reference, comparing it with the output through R26, R27 and the -5 V SENSE line at P103, pin 3. The -5 V output tracks the +5 V supply and potentiometer R19 adjusts both. Output current is limited by cutting the base drive to Q6 when the drop across R30 approaches one diode drop.



NOTES: (UNLESS OTHERWISE SPECIFIED)

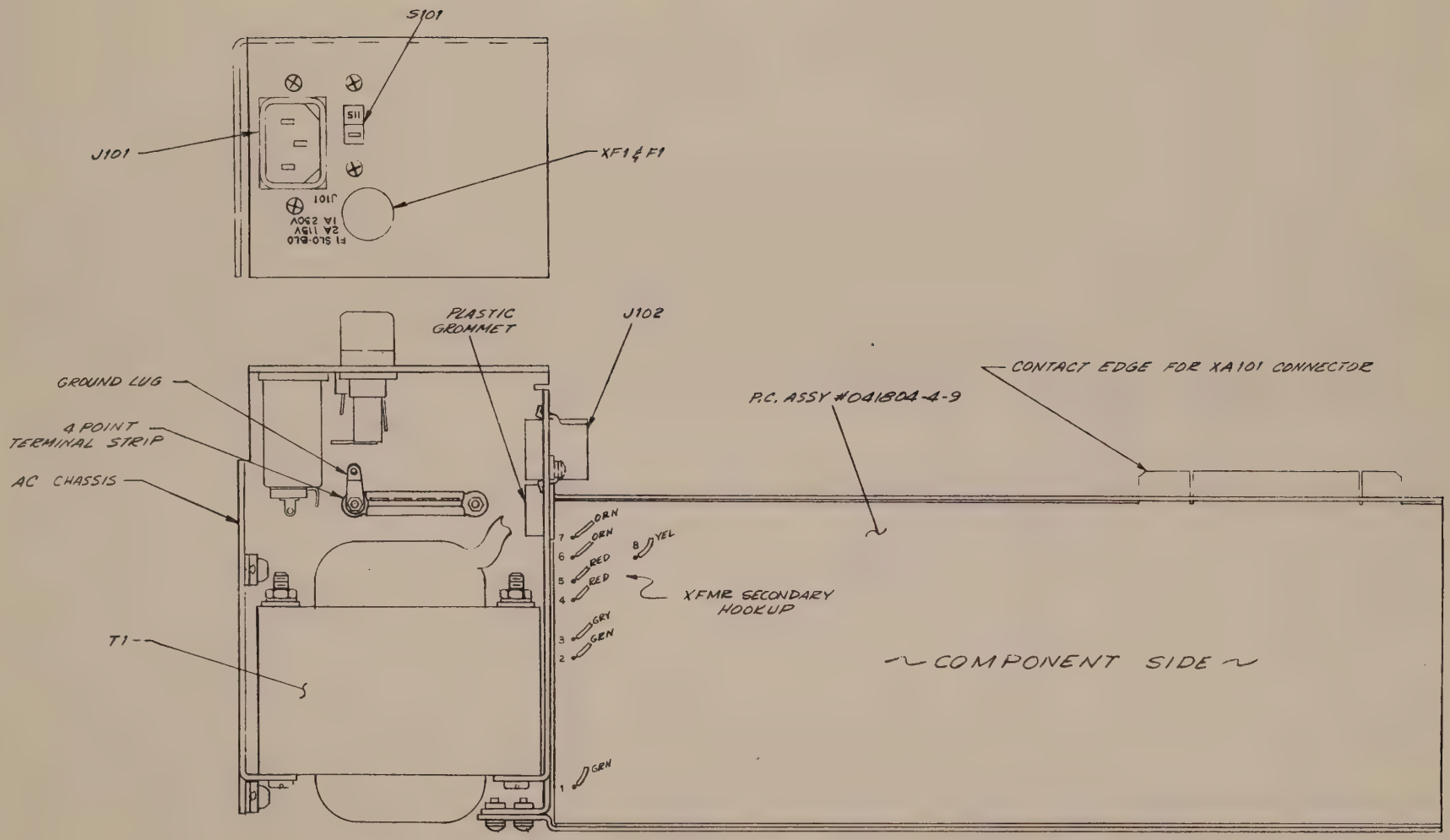
1. COMPONENTS OUTSIDE DOTTED AREA ARE PART OF AC CHASSIS ASSY 41810-4-9.
2. ○ INDICATES NUMBERED PAD ON PC ASSY 41804-4-1.
3. □ INDICATES PIN NUMBER OF XA101 EDGE CONNECTOR ON PC ASSY 41804-4-9.
4. ⬡ INDICATES TEST POINT.
5. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
6. ALL CAPACITORS ABOVE 1μf ARE ALUM. ELECTROLYTIC, CAPACITORS BELOW 1μf ARE CERAMIC DISC.
7. ALL DIODES ARE IN4005.
8. U1 & U2 ARE μA723PC. U3 IS μA747PC.



POWER SUPPLY

SCHEMATIC #041810-7-9 REV C,

8154-2-79



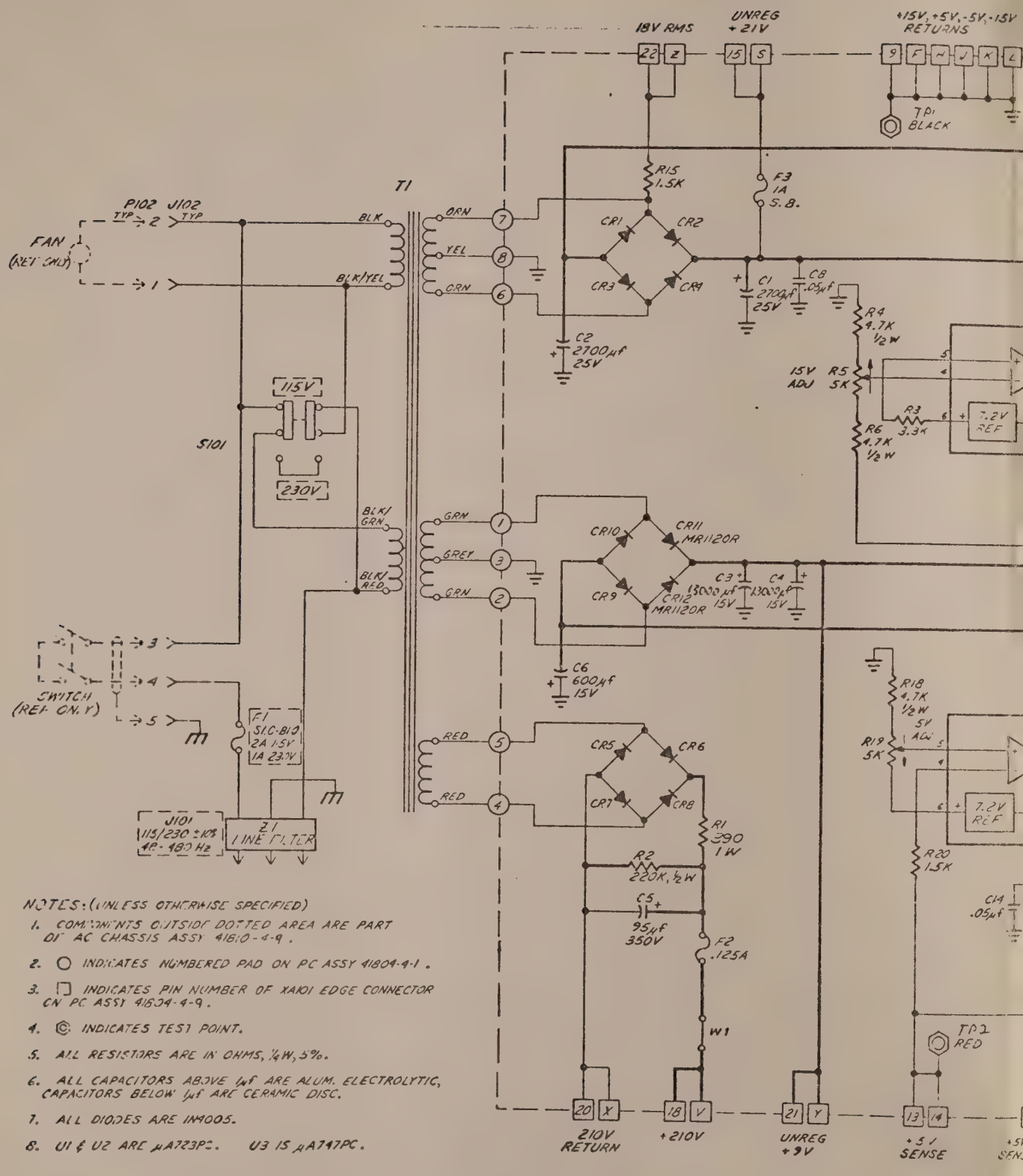
POWER SUPPLY ASSEMBLY #041810-4-9 REV A_3

5-93

PARTS LIST

POWER SUPPLY ASSEMBLY #041810-7-9

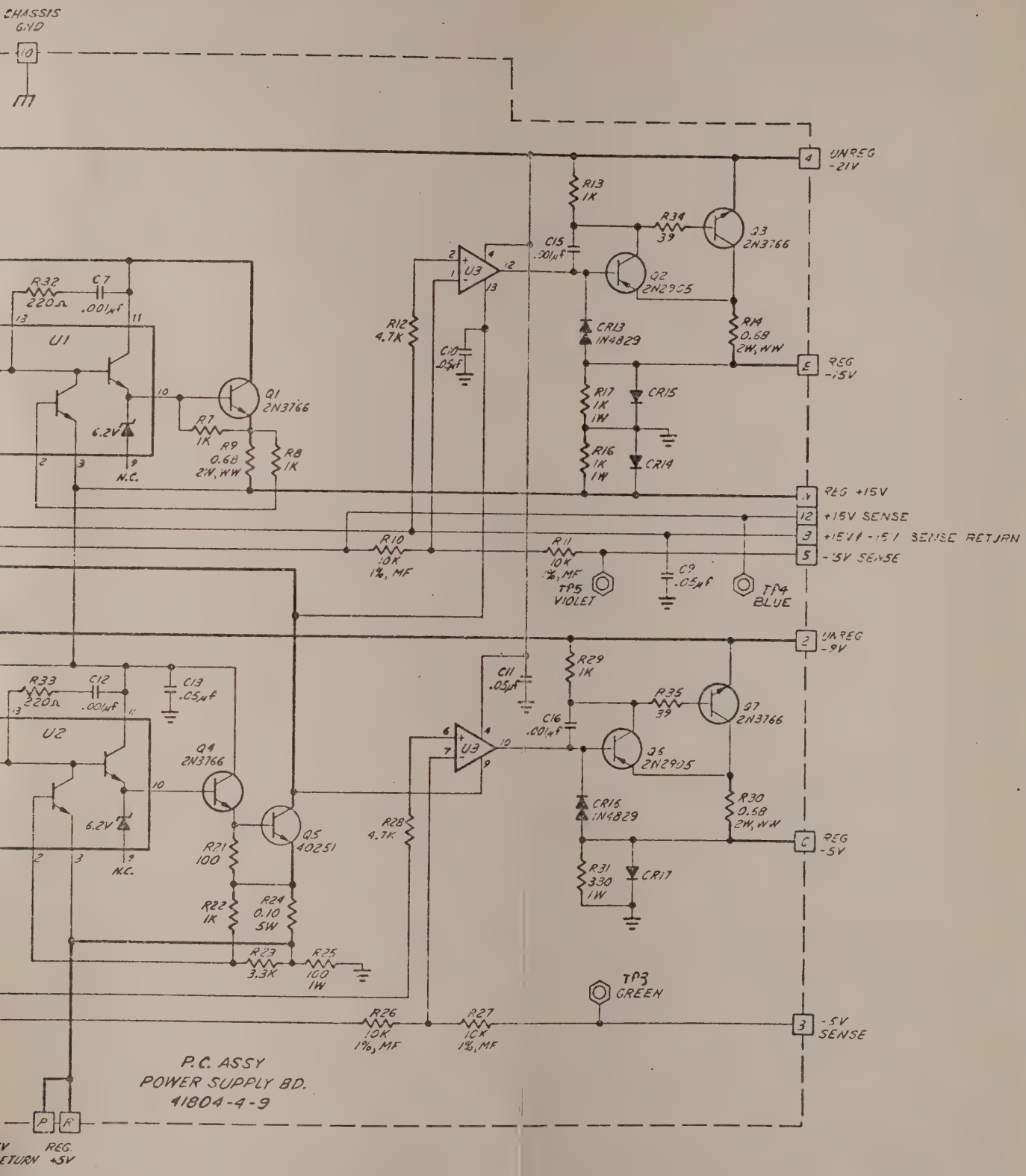
REF.	DESCRIPTION	SD PART NO.
	Assembly	041810-4-9
	Schematic	041810-7-9
	Assembly	041804-4-9
	Chassis	041810-1-6
J101/Z1	Filter Line/Power Input Connector	102461
XF1	Fuse post	102409
F1	Fuse, 2 A, Slo-Blo, 115 V	100585
S101	Switch, Slide (115/230)	102331
J102	Connector, Shell 5-contacts	101264
	Contact, Female	10282201
T1	Transformer	02140861
	Screw, 10-32 X 2.75 PHMS	10064444
	Washer, #10 Fiber	100684
	Strip, Terminal 4-point	100084



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENTS OUTSIDE DOTTED AREA ARE PART OF AC CHASSIS ASSY 41610-4-9.
2. ○ INDICATES NUMBERED PAD ON PC ASSY 41804-4-1.
3. [ ] INDICATES PIN NUMBER OF XA101 EDGE CONNECTOR ON PC ASSY 41604-4-9.
4. ⓒ INDICATES TEST POINT.
5. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
6. ALL CAPACITORS ABOVE 1μf ARE ALUM. ELECTROLYTIC, CAPACITORS BELOW 1μf ARE CERAMIC DISC.
7. ALL DIODES ARE IN4005.
8. U1 & U2 ARE μA723PC. U3 IS μA747PC.

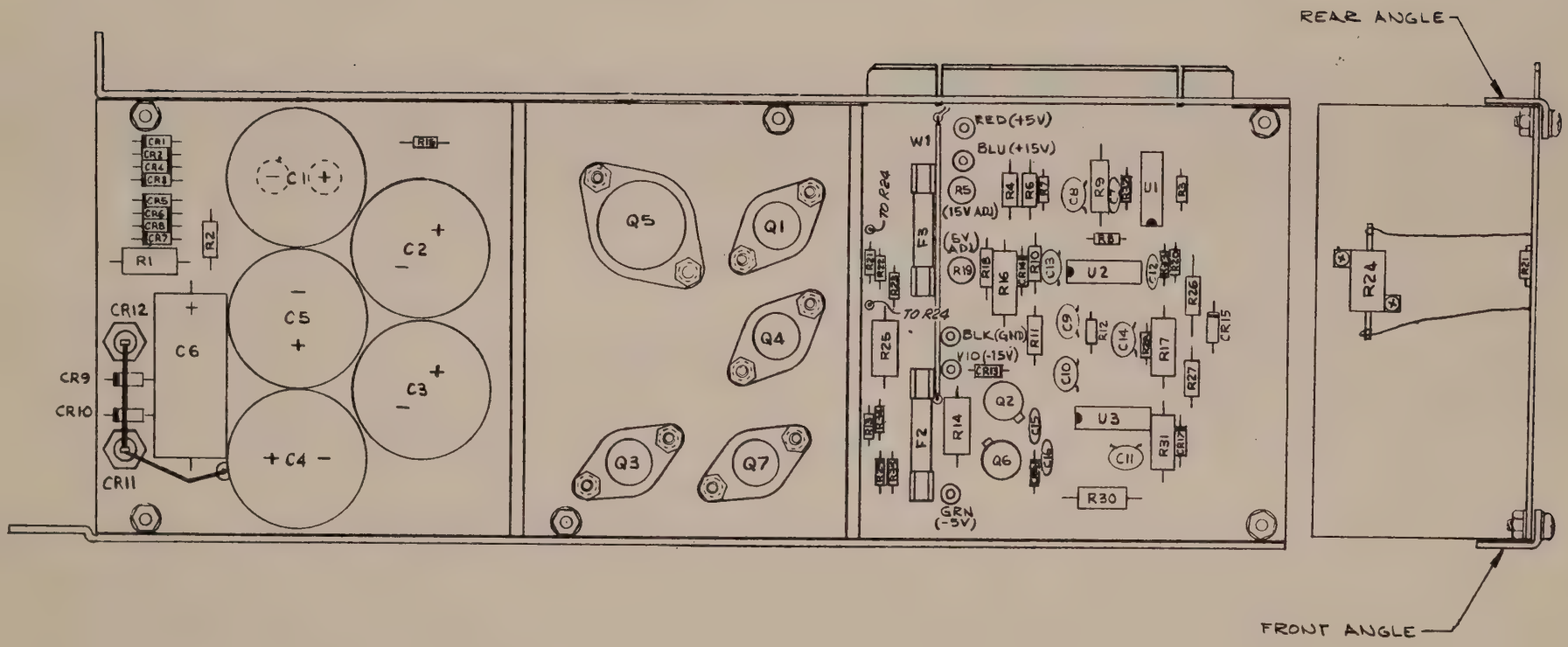
8154-6-76



POWER SUPPLY

SCHEMATIC #041810-7-9 REV C,

8154-2-79



POWER SUPPLY REGULATOR ASSEMBLY #041804-4-9 REV C

5-95 A

PARTS LIST

POWER SUPPLY BOARD #041804-4-9 (REV E)

REF.	DESCRIPTION	SD PART NO.
	Assembly	041804-4-9
	Schematic	041810-7-9
C1,2	Capacitor, 2700 µF, 25 V	100232
C3,4	Capacitor, 13,000 µF, 15 V	116074
C5	Capacitor, 95 µF, 350 V	100259
C6	Capacitor, 600 µF, 15 V	100258
C7,12,15,16	Capacitor, .001 µF, 1 kV, Disc	100076
C8-11,13,14	Capacitor, .05 µF, 50 V, Disc.	100134
CR1-10,14,15,17	Diode, 1N4005	100413
CR11,12	Diode, MR1120R	100424
CR13,16	Diode, 1N4829	100443
F2	Fuse, 3 AG, .125 A	100592
F3	Fuse, 3 AG, 1 A Slow Blow	100584
Q1,3,4,7	Transistor, 2N3766	101373
Q2,6	Transistor, 2N2905	101382
Q5	Transistor, 40251	101354
R1	Resistor, 390 k, 1 W, ±5%, CC	101532
R2	Resistor, 220 k, ½ W, ±5%, CC	101458
R3,23	Resistor, 3.3 k, ¼ W, ±5%, CC	101559
R4,6,18	Resistor, 4.7 k, ½ W, ±5%, CC	101511
R5,19	Potentiometer, 5 k	101859
R7,8,13,22,29	Resistor, 1 k, ¼ W, ±5%, CC	101569
R9,14,30	Resistor, .68 Ω, 2 W, ±5%, WW	101829
R10,11,26,27	Resistor, 10 k, ¼ W, ±1%, MF	101930
R12,28	Resistor, 4.7 k, ¼ W, ±5%, CC	101598
R15,20	Resistor, 1.5 k, ¼ W, ±5%, CC	101577
R16,17	Resistor, 1 k, 1 W, ±5%, CC	101635
R21	Resistor, 100 Ω, ¼ W, ±5%, CC	101609
R24	Resistor, 0.1 Ω, 5 W, ±1%, WW	102218
R25	Resistor, 100 Ω, 1 W, ±5%, CC	101856
R31	Resistor, 330 Ω, 1 W, ±5%, CC	101624
R32,33	Resistor, 220 Ω, ¼ W, ±5%, CC	101566
R34,35	Resistor, 39 Ω, ¼ W, ±5%, CC	101733
U1,2	Integrated Circuit, 723PC	025761
U3	Integrated Circuit, 747PC	045205
W1	Wire, 24 AWG Solid Teflon	
XF2,3	Socket, Fuse (clip)	116299
XQ1,3-5,7	Socket, Pin	102442
XU1-3	Socket, 14-pin, Augat	102433

PARTS LIST

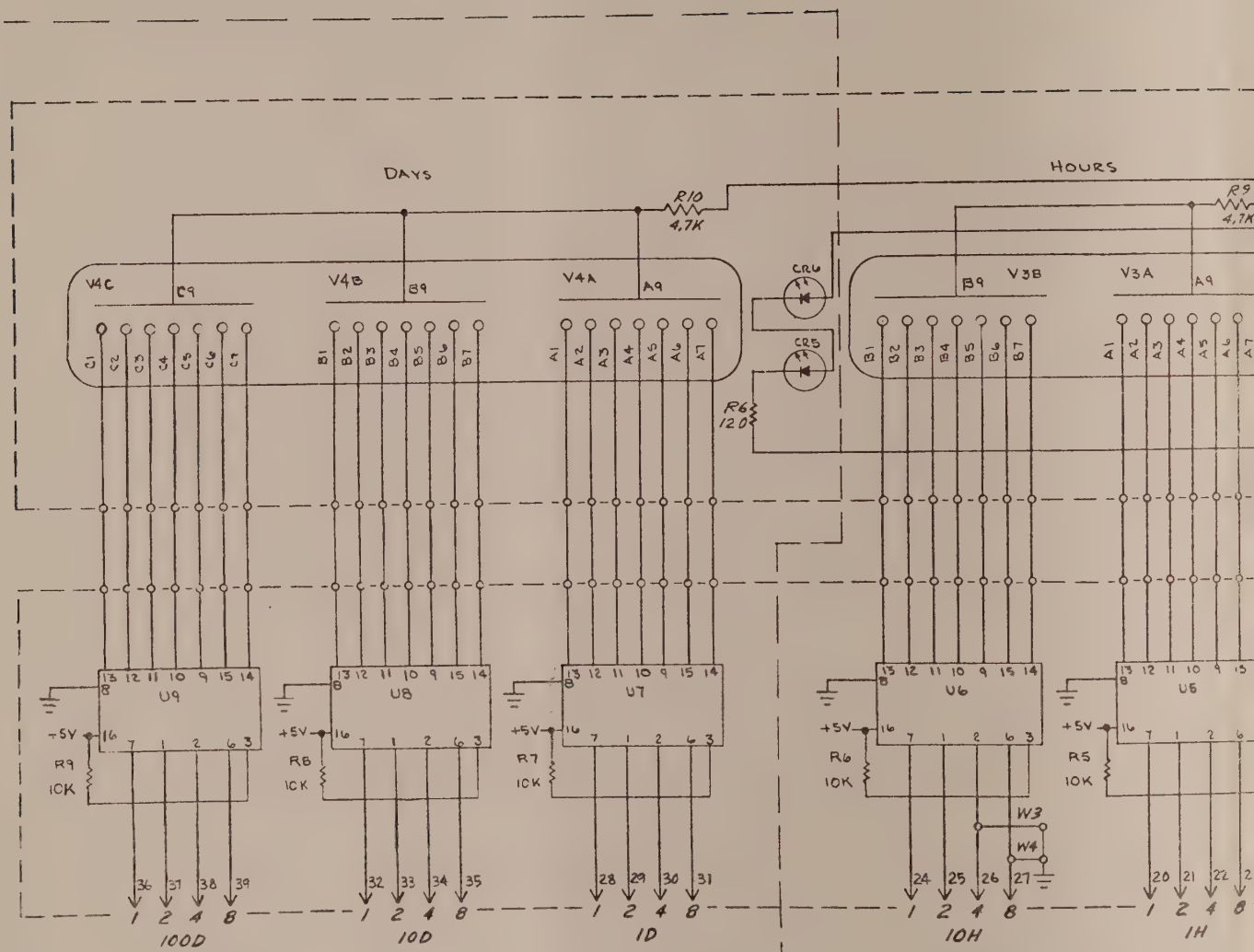
POWER SUPPLY BOARD #041804-4-9 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
	Test Point, Red, +5 V	100541
	Test Point, Black, Grd.	100542
	Test Point, Green, -5 V	100543
	Test Point, Blue, +15 V	100547
	Test Point, Violet, -15 V	100548
	Socket, Pin	103037
	Heatsink	041805-1-1
	Pad, Transistor	100666
	Transistor, Modification	051124-1-1
	Angle, Front	041811-1-2
	Angle, Rear	041812-1-2
	Heatsink, Assembly	041805-4-1
	Solder, Wave	041804-3-9

CIRCUIT DESCRIPTION
DISPLAY ASSEMBLY
SCHEMATIC #041945-7-2

1) GENERAL

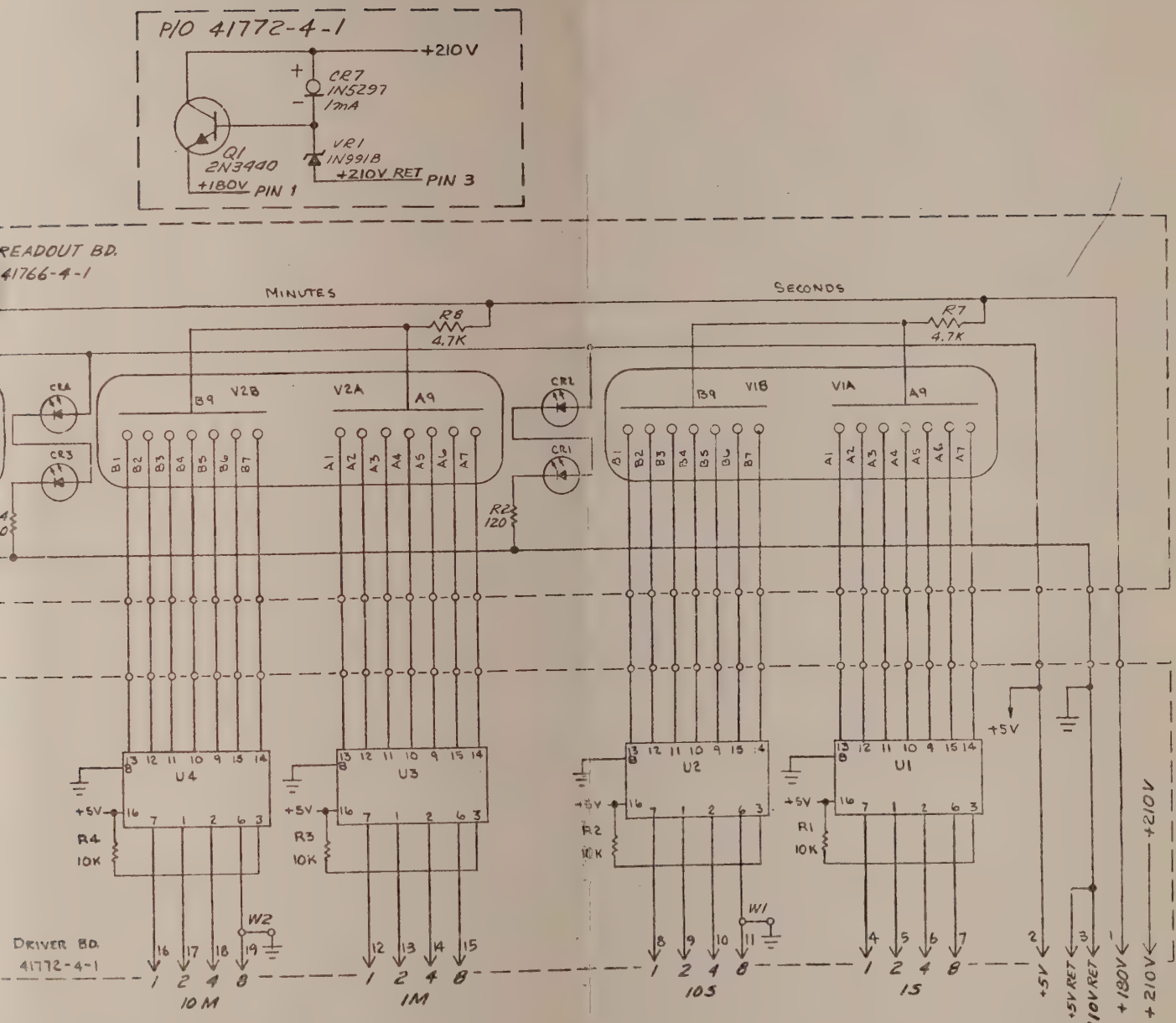
The basic display assembly has three 2-digit, in-line, planar indicator tubes and associated driver chips for the display of time in hours, minutes and seconds. LED colons are provided between the tubes. The assembly includes provision for the addition of a 3-digit days display plus a third colon when the Days Option is included. Time information is accepted in parallel BCD form.



NOTE:
THIS SECTION NOT USED FOR UNITS WITHOUT DAYS

NOTES: (UNLESS OTHERWI

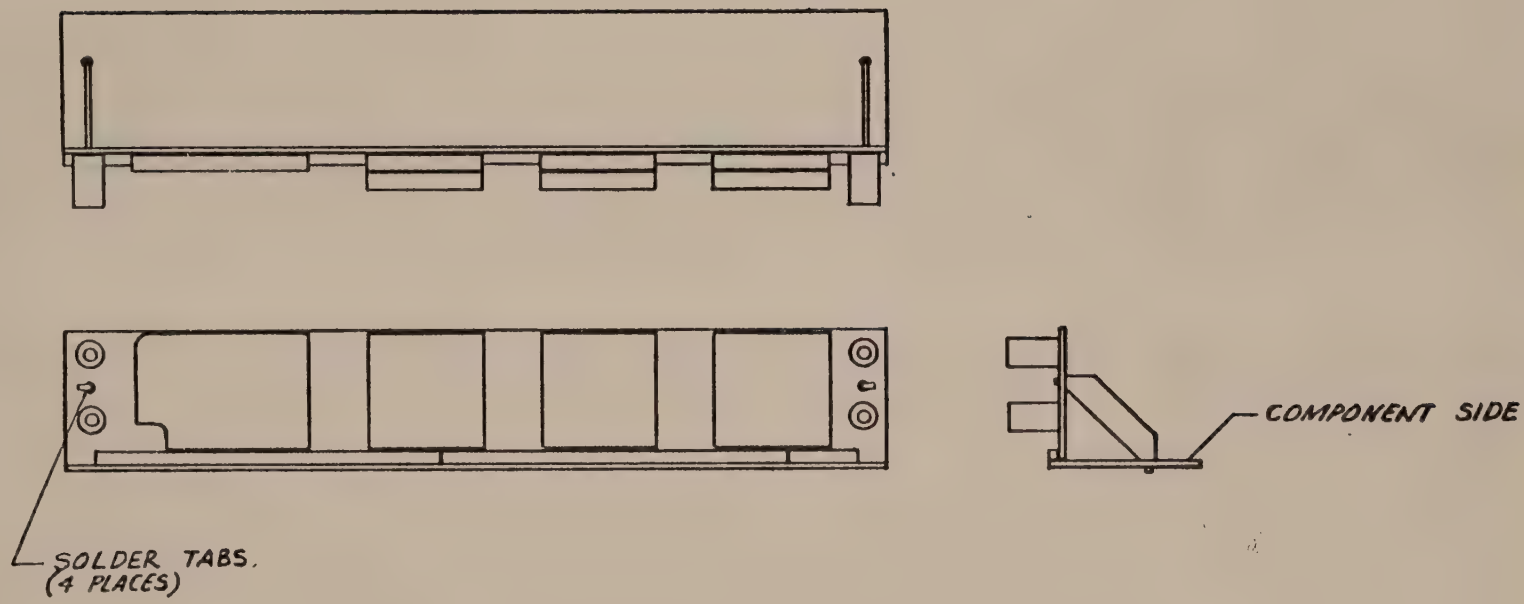
1. ALL RESISTORS ARE IN O
2. ALL DIODES ARE FLV-100.
3. ALL IC's ARE DD-700.



SPECIFIED)

5, ½ W, 5%.

READOUT & DRIVER
SCHEMATIC #041945-7-2 REV G

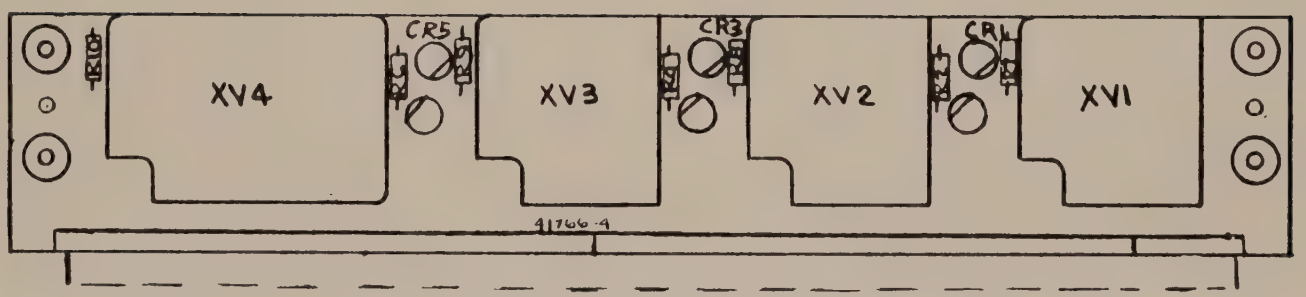


DISPLAY ASSEMBLY, 6 DIGIT #041945-4-2 REV E_1

PARTS LIST

6-DIGIT DISPLAY ASSEMBLY #041945-7-2

REF.	DESCRIPTION	SD PART NO.
	Assembly, Display & Driver	041945-4-2
	Assembly, Display	041766-4-1
	Assembly, Driver	041772-4-1
	Schematic	041945-7-2
V1-V3	Display Tube, SP-352 Sperry	102403
	Bracket, Display & Driver Board	051450



NOTE:
1.) CR 5 & 6 MOUNTED WITH DAYS OPTION ONLY.

DISPLAY BOARD, 9-DIGIT #041766-4-1 REV G_2

9-DIGIT DISPLAY DRIVER ASSEMBLY #041772-4-1 REV E

PARTS LIST

DISPLAY ASSEMBLY #041766-4-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	041766-4-1
	Schematic	041945-7-2
CR1-4,6	Lamp, LED	100455
R2,4,6	Resistor, 120 Ω, 5%, ¼ W	101717
R7-10	Resistor, 4.7 k, 5%, ¼ W	101598
XV1-3	Socket, Display 2-digit	102445
XV4	Socket, Display 3-digit	102446
	Spacer, LED Lamp	101077
	Spacer, Swage, 4-40X.437 large	101062
	Connector 30-Pin Right Angle	101277
	Connector Mod 6-Pin Right Angle	07189106

DRIVER ASSEMBLY #041772-4-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	041772-4-1
CR7	Diode, 1N5297	100457
Q1	Transistor, 2N3440	101420
R1-9	Resistor, 10 k, 5%, ¼ W	101570
U1-6,8-9	Integrated Circuit, Sperry #DD-700	045203
VR1	Diode, 1N991B	100461
W1-4	Jumper, Molded	102879
	Socket, 16-Pin DIP	103350

CIRCUIT DESCRIPTION
RELAY CHASSIS ASSEMBLY
SCHEMATIC #7-061400

1) GENERAL

The relay assembly consists of disconnect relays, K1 and Transport control relays K2, K3, K4, K6, K7 and K8.

The relay coils are driven by drivers in the Search Unit, Reader/ Search Unit, or Reader/Generator/Search Unit in which the Assembly is installed. The contacts are wired to J401, the Transport Control Connector, so that they may be wired to the Tape Transport as desired by the user (refer to Chapter 6, Drawings #041335-7-XX for recommended connections for most commonly-used Transports.

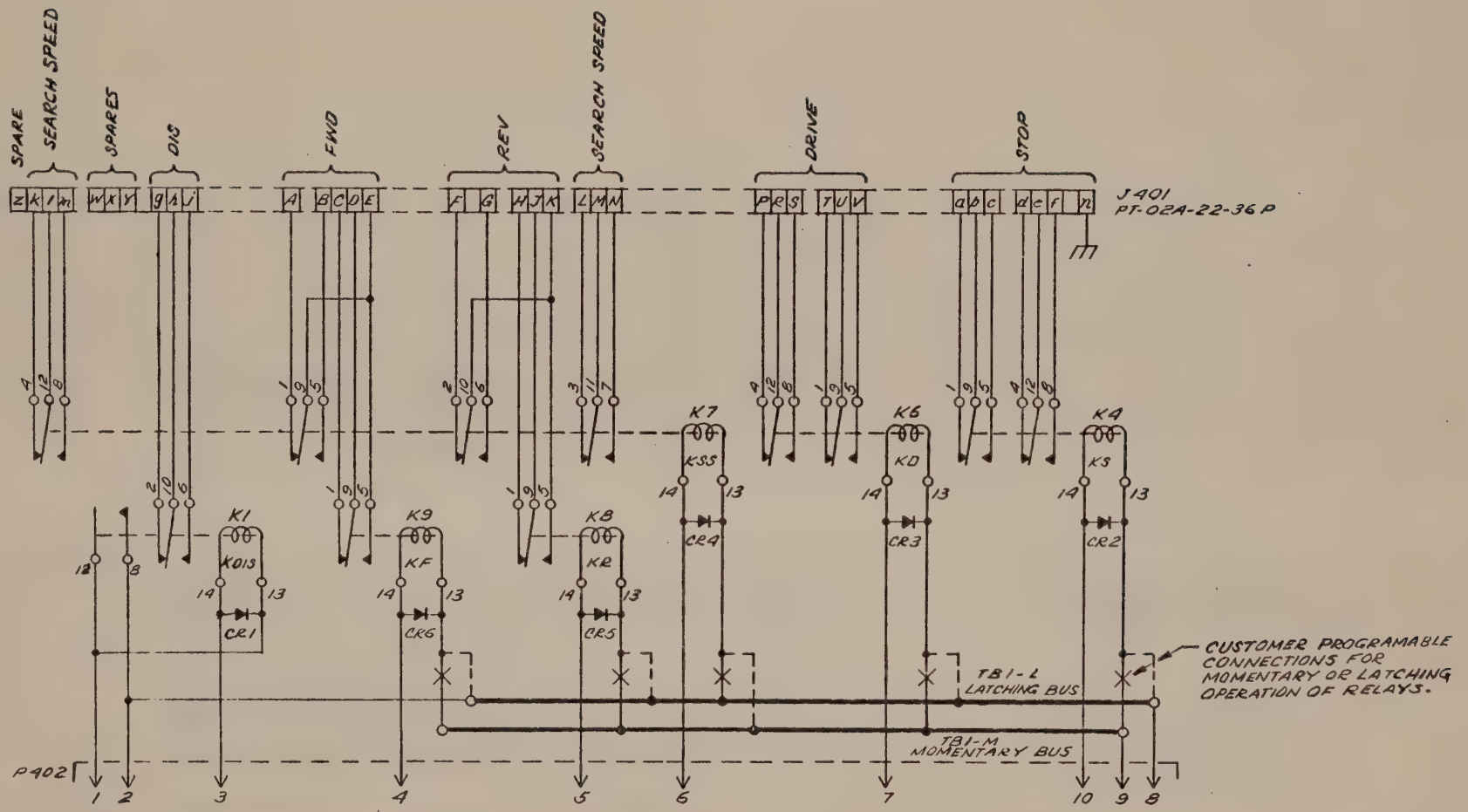
2) CIRCUIT DESCRIPTION

The Disconnect (KD1S) Relay, K1 is deenergized in the DISCONNECT and PWR OFF Modes and controls coil power to the 5 Transport Control Relays. "Form C" contacts are bought out on J401.

The 5 Transport Control Relays are: STOP (KS), K4; DRIVE (KD), K6; (fast) REV (KR), K8; (fast) FWD (KF), K9; and SEARCH SPEED (KSS), K7. The first 4 correspond to the front panel pushbuttons for the transport function, and K7 is actuated for both FWD and FEV functions. All 5 relays may be programmed for MOMENTARY or LATCHED operation. In LATCHED operation, a relay for a particular function is energized as long as that function is selected; in MOMENTARY, a relay is energized for approximately 140 milliseconds when a new function is selected. In either case, no two relays (except KF and KSS or KR and KSS) are energized, even momentarily.

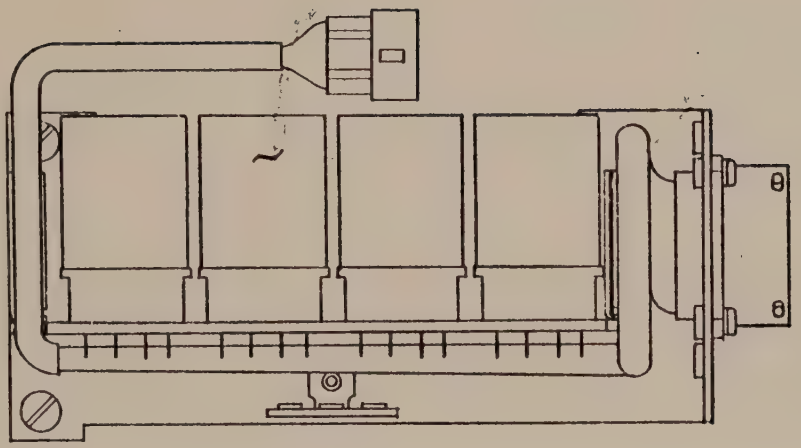
3) PROGRAMMING

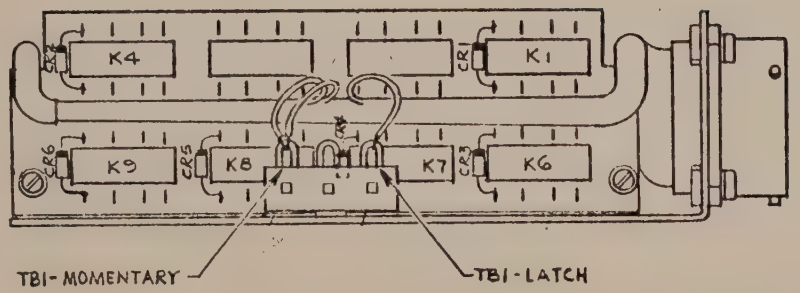
All transport control relays are factory programmed for MOMENTARY operation except KSS which is LATCHED. Reprogramming may be accomphished by removing the Relay Chassis Assembly. First remove the 4 screws securing it to the rear panel, then remove the 2 captive fasteners inside, near the card cage and lift out and disconnect P402. Refer to Schematic #7-061400, noting the wire colors for pin 13 of the relay of interest, and to Assembly drawing #05191502 for the location of the MOMENTARY and LATCH bus lugs. Use a small soldering iron to make the desired chage. Reinstall the Relay Chassis Assembly and check for desired operation.

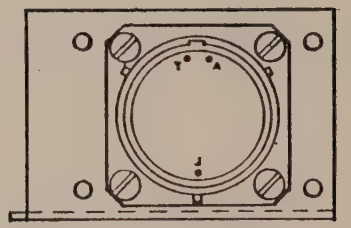


NOTE: UNLESS OTHERWISE NOTED;
1.) RELAYS — KHP-110 II 24 V.
2.) DIODES — IN4151.

RELAY CHASSIS SCHEMATIC #7-061400 REV A_1







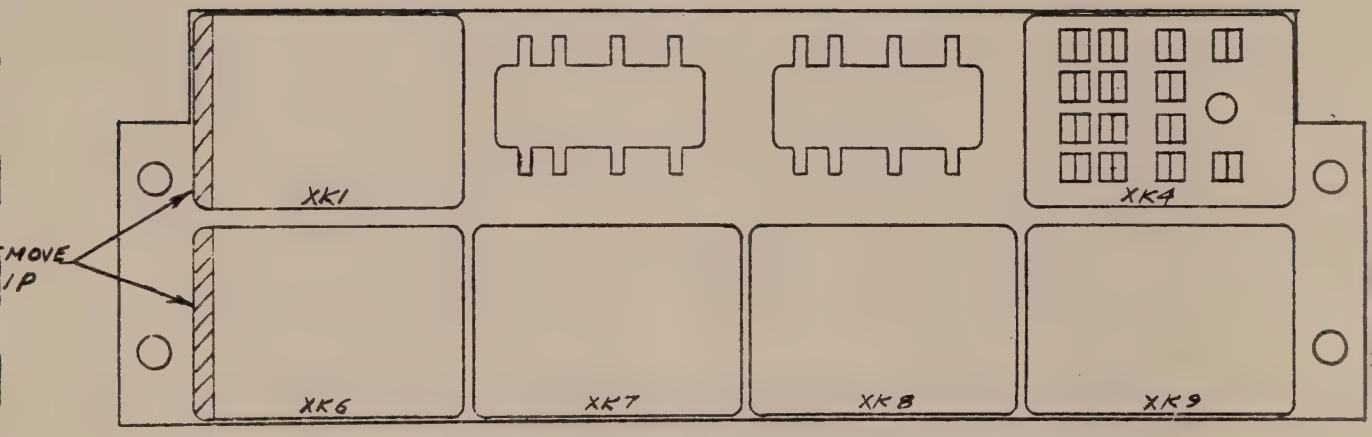
CONNECTOR ORIENTATION

RELAY CHASSIS ASSEMBLY #06137401 REV B

PARTS LIST

RELAY CHASSIS #06137401 (REV C)

REF.	DESCRIPTION	SD PART NO.
	Assembly	06137401
	Schematic	7-061400
	Assembly, Relay Board	05191502
CR1-6	Diode, 1N4151	100385
J401	Connector, PT-02A-22-36P	101211
K1,4,6-9	Relay, 24 V	101290
P402	Connector, 12-pos	102808
	Pin, Terminal 1560	10282202
	Bracket Insulation	061382



RELAY BOARD ASSEMBLY #05191502 REV C

PARTS LIST

RELAY BOARD #05191502 REV B

REF.	DESCRIPTION	SD PART NO.
	Assembly	05191502
XK1,4,6-9	Relay, Socket	102417

CHAPTER 6
STANDARD OPTIONS

6.1 GENERAL

Several standard options are available for the Model 8154. All options, when supplied with the instrument, will be described on the following pages.

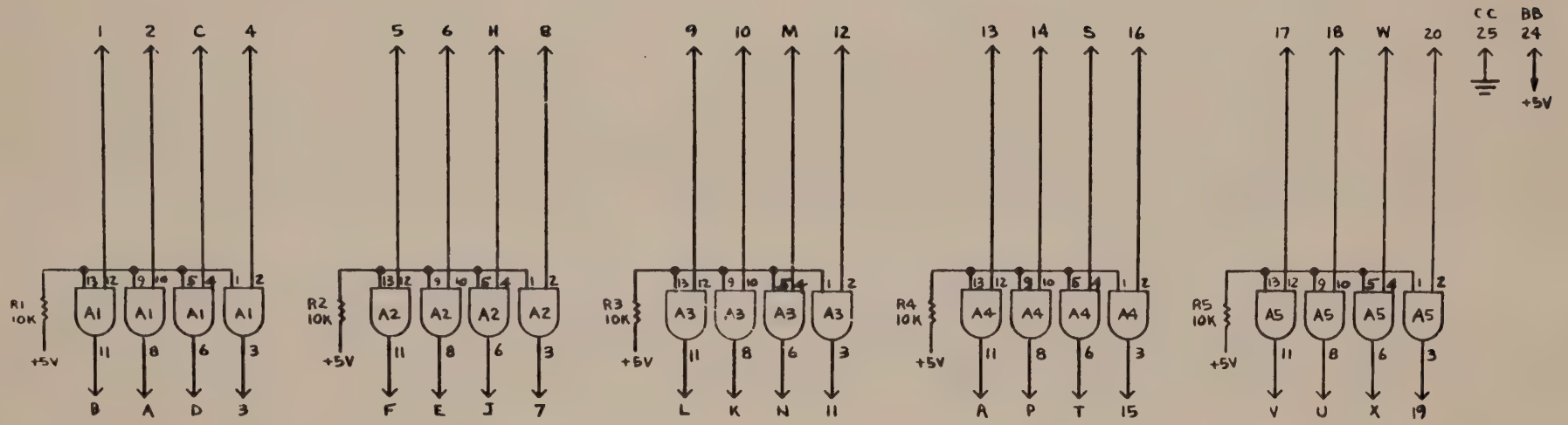
PARTS LIST
OPTION D15/D15A - #06133107 REV A

REF	DESCRIPTION	SD PART NO.
	ADD	
	Schematic (Block Diagram 8154)	7-05192905
A16	Assembly, Buffer	021535-4-3
J3	Connector, 50-Conductor, 57-40500	101156
P3	Connector, 50-Conductor, 57-30500	101157
XA16	Connector, 50-Conductor	101204
	Card Guide	
	DELETE	
J3	Cover Plate	031394-1-1

CIRCUIT DESCRIPTION
BUFFER
SCHEMATIC #021535-7-3

1) GENERAL

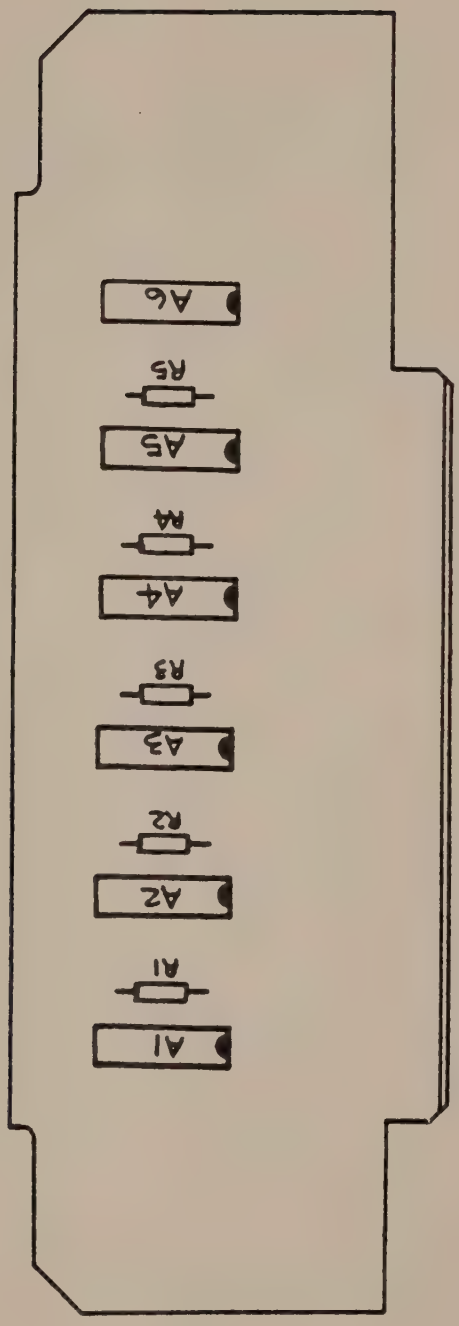
This card contains twenty integrated-circuit gates, connected as non-inverting buffers. It is used to buffer the seconds through hours outputs of the Time-of-Day Accumulator. A binary "1" output is 5 V (±0.5 V) 6 kΩ source. A binary "0" output is 0 V (±0.5 V) 15 mA sink.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V & PIN 7 " " " " " " GND.
3. A1 THRU A5 ARE MC1806P

BUFFER SCHEMATIC #021535-7-3 REV A.



BUFFER ASSEMBLY #021535-4-3

PARTS LIST

BUFFER ASSEMBLY #021535-4-3

REF.	DESCRIPTION	SD PART NO.
	Assembly	021535-4-3
	Schematic	021535-7-3
A1-5	Integrated Circuit, MC1806P	025733
R1-5	Resistor, 10 k 5%, 1/4 W	101570
W1-5	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
DAYS/ID (OPTIONS E13/D15A)
BLOCK DIAGRAM #7-05192905

1) GENERAL

The Days/ID Option is shown on the instrument Block Diagram. This option adds the #021632-2-21 Days Accumulator (A28), #021501-4-1 Comparator (A22), Preset thumbwheel switches S7-S9 and S19-S21, a colon and three-digit display to Display Assembly A102 and the associated wiring.

A three-position switch (S33) is added to the rear panel to allow selection of 365 (Days), 366 (Days with Leap Year), or ID (Identification or Run Number). When ID is selected, a range of 000 to 999 is possible, and the ID number may be externally updated by application of a negative DTL/TTL level transition to the UPDATE BNC (J13) on the rear panel. A contact closure may also be used, but filtering must be used to eliminate the effects of contact bounce.

2) PARALLEL OUTPUTS (OPTION D15A)

Parallel BCD Days/ID outputs are supplied to connector J3 through buffers on the Days Accumulator card when Option D15A is included. These 12-bits have the following specifications:

Code: 8-4-2-1.

Logic: "1" = +5 ±0.5 V behind 6 kΩ.

"0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

PARTS LIST

DAYS/ID OPTION (E13) #06131614 REV A_1

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-05192905
A21	Assembly, Days Accumulator	021632-4-21
A22	Assembly, Comparator	021501-4-1
CR5,6	Lamp, Led	100455
J13	Connector, BNC	101155
S7-9,19-21	Switch Assembly, Thumbwheel	05130001
S33	Switch, Slide	102632
U7-9	Integrated Circuit, DD700	045203
V4	Display, SP353	102404
XA21,22	Connector, PC Edge, 50-Contact	101204
	Eyelet (for S33)	112482
	Spacer, Led	101077
	Guide, Card	021340-1-2
	Insulator	100823
	DELETE	
J13	Hole Plug, BNC	100952
S33	Cover Plate, Slide Switch	05120802
	Spacer, Thumbwheel Switch	102358

CIRCUIT DESCRIPTION
DAYS ACCUMULATOR
SCHEMATIC #021632-7-21

1) GENERAL

The Days Accumulator Card can provide up to 3 serial decades with common reset, parallel preset and 2 sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. A days recycle circuit is included which may be programmed to reset the accumulator to 001 at the end of 365 or 366 days.

2) DECADE DIVIDERS

The up to 3 decade dividers are connected in tandum. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through 2 sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the 2 sets (A10, A13 and A15) can be gated by inputs through pins L,K and J, respectively. These gate lines are buffered by inverters A11.

4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8,11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

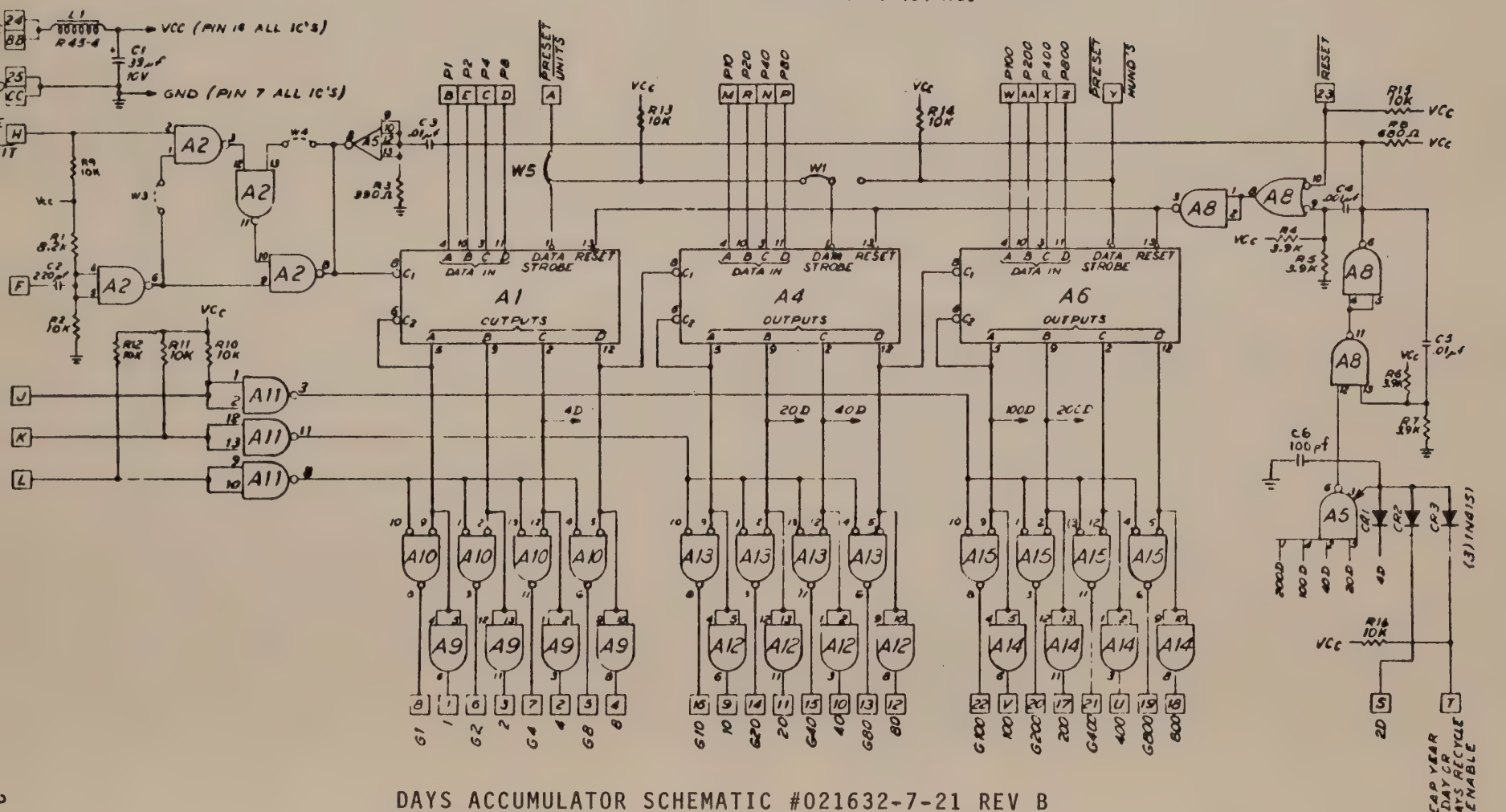
5) DAYS RECYCLE CIRCUIT

Gate 5-6 is a 4-input NAND gate with an expander input. The connection of diodes CR1-CR3 gives the gate 7-inputs. If recycle at 366 is desired, pin T is connected to Vcc. If recycle at 367 (for leap year) is desired, pin T is connected to pin 1 (the one day output). Pin S is always connected to the 2 day output. At the selected count, the output of A5-6 will go low, triggering one-shot A8-11,6. The one-shot output is a negative-going pulse (from +5 to 0 V). The leading edge of the pulse (ac-coupled into A8-8) causes the 3 dividers to reset to 000. The trailing edge of the pulse (which is positive-going) is ac-coupled into A5-8 where it is inverted and used to input 1 count to the first decade. The resulting accumulator contents are 001.

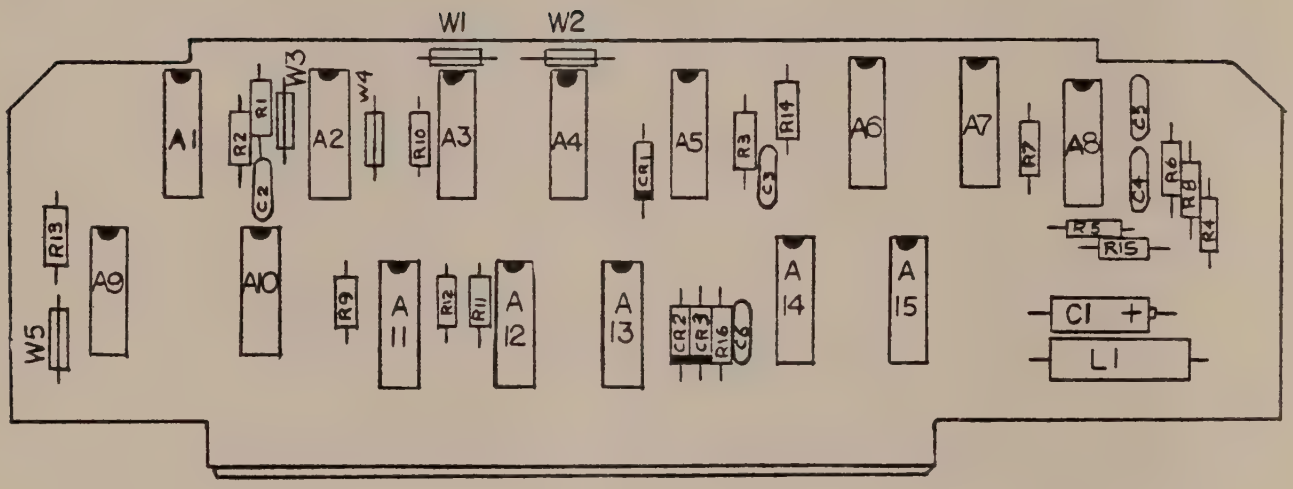
NOTES:
1. INT. CKT. TYPES AS FOLLOWS:
A1,4,6 = N8280P.
A2 = MC846P

A5 = MC830P.
A8 = SN7400N.
A9,12,14 = MC1806P.
A10,13,15 = MC1808P.

A11 = MC846P.
2. C3 USED FOR DAYS RECYCLE TO "1".
3. FOR TENS TO PRESET WITH UNITS INSTALL W1 AND NOT W2.



DAYS ACCUMULATOR SCHEMATIC #021632-7-21 REV B



DAYS ACCUMULATOR ASSEMBLY #021632-4-1 REV C

PARTS LIST

DAYS ACCUMULATOR #021632-7-21 REV B

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #021632-4-1)	021632-4-21
	Schematic	021632-7-21
A1,4,6	Integrated Circuit, N8280P	025722
A2,11	Integrated Circuit, MC846P	019716
A5	Integrated Circuit, MC830P	019712
A8	Integrated Circuit, SN7400N	019705
A9,12,14	Integrated Circuit, MC1806P	025733
A10,13,15	Integrated Circuit, MC1808P	025734
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF, Disc	100044
C3,5	Capacitor, .01 µF, Disc	100103
C4	Capacitor, .001 µF, Disc	100076
C6	Capacitor, 100 pF, DM	100173
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1	Resistor, 8.2 k, 5%, 1/4 W	101595
R2,9-16	Resistor, 10 k, 5%, 1/4 W	101570
R3	Resistor, 390 Ω, 5%, 1/4 W	101592
R4-7	Resistor, 3.9 k, 5%, 1/4 W	101601
R8	Resistor, 680 Ω, 5%, 1/4 W	101669
W1,5	Jumper, Molded	102879
	Extractor	100865

PARTS LIST
OPTION E14 - SEARCH TO MILLISECONDS #06128803 REV A

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic (Block Diagram 8154)	7-05192905
C2	Capacitor, 3300 pF 20%, 200 V	100153
R9	Resistor, 8.2 K 5%, 1/4 W	101595
R12	Resistor, 10 K 5%, 1/4 W	101570
S10-12,22-24	Thumbwheel Switch (S10,22 P/N 051374)	05130001
	DELETE	
	Switch Spacer	102358
	Trim Strip Insert	041774-1-1

CIRCUIT DESCRIPTION
BCD MILLISECONDS (OPTION E14A)
BLOCK DIAGRAM #7-05192905

1) GENERAL

The BCD Milliseconds option is shown on the basic unit Block Diagram, Drawing #05192905. This option adds 14-pin rear panel connector J6 and associated wiring.

Parallel BCD Milliseconds outputs are supplied to J6 from buffers on Minor Counter card A9. These 12 bits have the following specifications.

Code:	8-4-2-1.
Logic:	"1" = +5 ±0.5 V behind 6 kΩ. "0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

PARTS LIST

E14A OPTION #06128911 REV A

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic (Block Diagram 8154)	7-05192905
J6	Connector, 14-Contact 57-40140	101180
P6	Connector, 14-Contact 57-30140 (Ship with)	101181
	DELETE	
J6	Cover Plate	021398-1-1

CHAPTER 7
SPECIAL MODIFICATIONS

7.1 GENERAL

Modifications to the Model 8154, requested by the customer, are documented in this chapter. These are usually extra-cost items to tailor the unit for a specific application.

CIRCUIT DESCRIPTION
REMOTE SPEED SELECTION (OPTION E16)
SCHEMATIC #7-07160608

1) GENERAL

This modified version of Option E16 is designed to provide remote selection of drive speed for the Ampex PR2200.

2) CIRCUIT DESCRIPTION

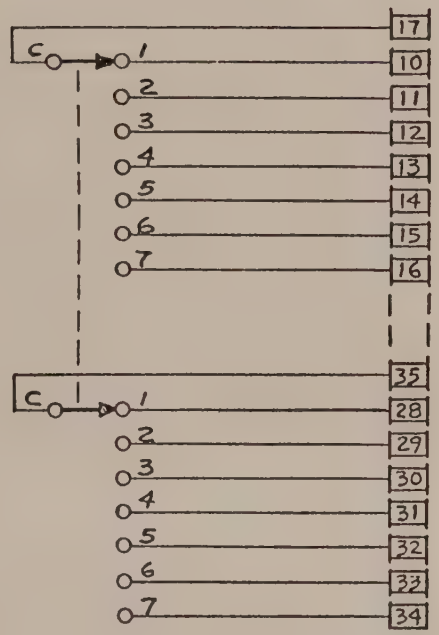
The option consists of a 2 pole, 7 position rotary switch (S52) wired to rear panel connector J7. External connections to the Ampex PR2200 are shown on Schematic #04149204. Both the Search Speed (K7) and the Stop (K4) relays are programmed for latched operation.

As shown at the bottom right of Schematic #7-07160608, a wiring change was made to DRIVERS Card connector XA26 to extend the Search Speed relay operate time to include the Stop Delay period.

REV	DESCRIPTION	SER NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS			1/2,	
B	"552" WAS "537". (REREL.)	-	←	1/17	[illegible]
B1	DELETED ---(7-051929) FROM NOTE 1.	-	NEC	1/17	

DRIVE SPEED
15/16
1 7/8
3 3/4
7 1/2
15
30
60

S52



P/O J7
(AMPHENOL # 57-40360 REF.)

A25-R —SD→ V P/O A26 DRIVERS 18 W → J402-6

NOTES:

1. THE CIRCUITRY SHOWN IS SUPERIMPOSED ON THE BASIC UNIT BLOCK DIAGRAM.
2. CONNECTOR J7, P.C. CARD A26 AND WIRE FROM A26-W ARE PART OF BASIC UNIT.

(AMPEX PR2200)

ITEM NO	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

PROPRIETARY DATA
Furnished under United States Government Contract No. ... It shall not be published nor disclosed outside the Government or used for any purpose except as specifically authorized in writing by Ampex Corporation. Ampex Corporation grants permission to the Government to duplicate this data for its emergency repair or overhaul work to the extent necessary to the performance of the work under the Government contract, but no right is granted to use this data for the purpose of duplication or manufacture of the item or process concerned or to disclose it to any person other than the Government performing the work under the contract. This restriction does not limit the right to use information contained in this data if it is obtained from another source without restriction. The limitations governing use of this data shall be indicated by this notice and by the marking of any reproduction hereof, in whole or in part.

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES / DECIMAL TOLERANCE .X ±.03 .XX ±.010 ANGLES ±	AMPEX CORPORATION CONCORD, CALIFORNIA
CHECK	DATE		
ELECT	DATE		CODE IDENT 52542
MECH	DATE		
QA	DATE		
MATERIAL P/L		SCALE	DO NOT SCALE DRAWING
SIZE D	DWG NO 07160608	REV B1	SHT 7 OF 7

REMOTE SPEED SELECTION (E1S OPTION)

APPLICATION

PARTS LIST
REMOTE SPEED SELECTION (OPTION E16)
SCHEMATIC #7-07160608

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-07160608
S52	Switch, Rotary	06134407
	Knob	102954
	Panel, Nomen	05193619
	DELETE	
	Panel, Nomen	051936

CIRCUIT DESCRIPTION
DAYS/ID (Option E13/E17A)
BLOCK DIAGRAM #7-061630

1) GENERAL

The Days/ID Option is shown on the instrument Block Diagram. This option adds the #21632-4-21 Days Accumulator (A21), Preset thumbwheel switches S12-S14, Leap Year/ID switch S33, and the associated wiring.

An ID Update input (IC levels) to rear panel BNC connector J13 is provided. This input is fed to a circuit on the Modulator A20.

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS QTY	SHT QTY
1	X	06163008	ASSY., OPTION E17	(NOTE 2)	X			
2		06103108	ASSY., MODEL 8134		1			
			DELETE					
5	X	06114201	NOMEN PANEL	C061142	1			
7	X	05120801	COVER PLATE (SLIDE SW.)	S32 (A051208)	1			
8		100952	HOLE PLUG (BNC)	J9	3			
9			" "	J10 S/A J9				
10			" "	J12 " "				
			ADD					
15			SCHEMATIC	7D06163008	REF.			
17	B	07103608	NOMEN PANEL MARKING		1			
18	C	06114211	NOMEN PANEL		1			
19			NOMEN PANEL SILKSCREEN	2D06163005	REF.			
21	B	06134413	SWITCH ASSY., ROTARY	S50 (NOTE 1)	1			
22		10231803	WAFER, "	S30B	2			
23			"	S30C S/A S30B				
24		102323	, TOGGLE	S49	1			
25		102954	KNOB		1			
26		100893	DRESS NUT		1			
29	B	021340-1-2	CARD GUIDE		10			
30		101204	CONNECTOR, P.C. EDGE	XA7	5			
31				XA8 S/A XA7				
32				XA14 " "				
33				XA20 " "				

REVISIONS

REV	DESCRIPTION
A	RELEASE TO RECORDS 1-22-79 KH
B	ADDED CRS & CR6. ECO 11681. 5-21-79. [illegible] 5/79
C	ECO 17205. K 10-12-80 [illegible]

NOTE:
1) PWR SW. IS MOVED FROM S30 TO S50.
2) THIS OPT. IS ADDED TO STD. MODEL 8134 TO MAKE AN 8154 W/E17.

JOB NO	LOT QTY	LOT NO.	CODE IDENT
			52542

PLANNER — PREP Bill DATE 01/19/79 — CHK'D — MAT. DUE — APP'D [illegible] — B/U REQ. — B/U COMP 8154-E17 — USED ON

SYSTRON DONNER CORPORATION

OPTION E17
ASSY. P/L

DRAWING NO.

SIZE	PART NO.	REV
P	06163008	C

SHEET 1 OF 2

FORM EB A 75

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
34			CONNECTOR	XA27 S/A XA7				
35		0006700	DIODE, 6700	CR5	4			
36			"	CR6 S/A CR5				
37			"	CR14				
38			"	CR15				
39		101569	RESISTOR, 1K, ¼W, 5%	R3	2			
40			"	R4 S/A R3				
42		102630	SWITCH, SLIDE	S32	1			
43		101155	CONNECTOR, BNC	J9	3			
44			"	J10 S/A J9				
45			"	J12 " "				
46		100823	INSULATOR, BNC		3			
47		101074	FIBER WASHER		3			
49		021554-A-1	P.C. ASSY., D C CODE GEN	A7 SEP P/L	1			
50		021543-4-3	TOD ACCUM	A8 " "	1			
51		021556-4-5	MODULATOR	A14 " "	1			
52		021632-4-2	MINOR COUNTER	A20 " "	1			
53		021566-4-15	TIME BASE	A27 " "	1			

REVISIONS

REV	DESCRIPTION

JOB NO.	LOT QTY	LOT NO.	CODE IDENT
			52542

PLANNER

PREP DATE: BILL 01/19/79

CHK'D

APP'D

MAT. DUE

B/U REQ.

B/U COMP

B154-E17

USED ON

SYSTRON DONNER CORPORATION

OPTION E17
ASSY. P/L

DRAWING NO.

SIZE	PART NO.	REV
P	06163008	C

SHEET 2 OF 2

FORM EB-A 75

CIRCUIT DESCRIPTION
CODE GENERATOR
SCHEMATIC #021554-7-1

1. GENERAL

The IRIG DC Code Generator card can be used to generate the IRIG A, B, C, E, or H codes. Code selection may be remotely controlled or fixed by the particular card configuration. Days information may be optionally included and provision is made for the insertion of control function bits and/or straight binary seconds from a source external to the card. The following description is intended to apply in general to all configurations of the card. The specific assembly used is identified by the attached assembly, schematic and parts list.

2. DIVIDER CIRCUITS

Refer to the timing diagrams and the schematic for this and subsequent sections. Divider A8 is a divide-by-two, then-by-five counter which divides down the "Z RATE" and provides decoded outputs for the code generating gates. Divider A15 is a divide-by-five, then-by-two counter which takes the output of A8, divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A17 is a divide-by-two, then-by-six counter. Its principle function is to control the secondary scan gate A4. The divide-by-twelve is used only for IRIG C, the divider being reset at the count of ten or by the sync input for the other codes. This early reset is shown on the timing diagram as A18-8. The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on Sheet two is simply eliminated when the divider resets at ten. Reset at ten is established by gate A18-8. A one-shot (A18-12,6) performs code frame reset. The external reset signal (pin Z) may be used for code frame reset when W1 is installed, or the card can supply a reset pulse to synchronize the associated accumulator when W2 is installed.

Divider A7 (if present) is a divide-by-five counter provided for external use. It is synchronized with the other divider chips.

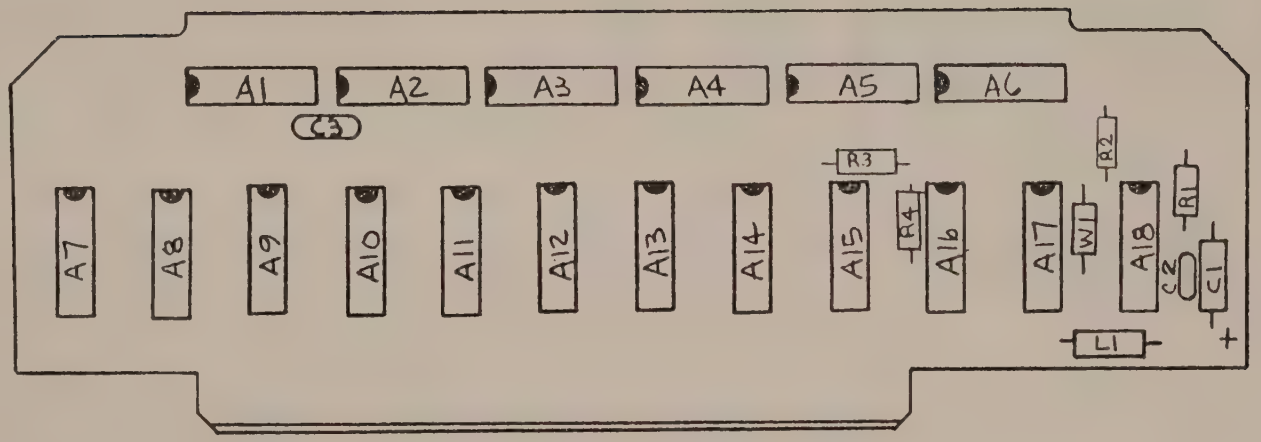
3. SCAN GATES

Creation of serial ONES is accomplished by a two-stage switching network and a series of gates. Chips A10-A14 are basically single pole (pin 8 is the output), 8-position switches. The inputs to these switches are the time data from the system accumulator. (One or more of these chips may be deleted on a particular card configuration.) The switching is controlled by BCD information on pins 1, 2 and 13. Since the above switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus, the need for switch A4. This switch, controlled from the BCD outputs of divider A17, selects the proper time interval for serializing each switch output. (The series of gates associated with A14 and A13, if present, further control these switches which may have outputs that should not be present in certain codes.) For example, tenths-of-seconds are added only in IRIG A, units-of-seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A5-8, A5-11 and A3-8 are used to inhibit the presence of serial ONES at certain times when no serial ONES should be present. This prevents the spurious ONES (coming from the switches) from appearing in the output code.

4. CODE GENERATING GATES

These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin 2. A "2" length is a ZERO, a "5" is a ONE, and an "8" is an INDEX MARKER.

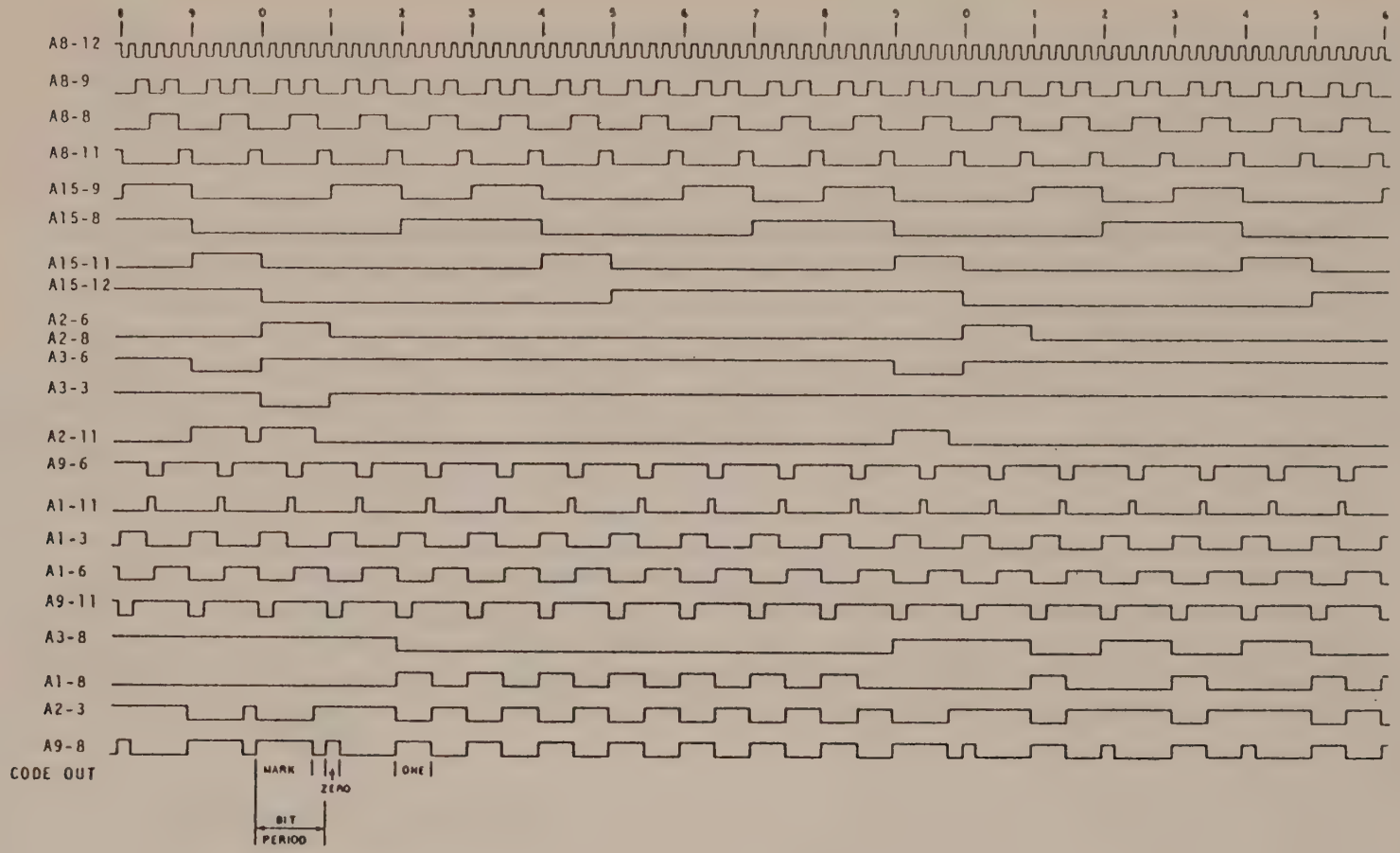
The INDEX MARKERS are generated by gating the output of divider A15. Gate A1-3 adds information from the output of divider A11 to create the "8" width. Gates A6-8 and A6-11 allow an extra pulse from gates A2-6 and A2-8 to give the "double mark" at the start of the frame. Gate A3-6 provides the marker at each tenth frame interval. Gate A9-11 supplies a pulse of "2" width at the start of each bit interval. If a MARKER or a ONE is not present, then the output code will be high for only the "2" width. Gate A1-6 supplies the "5" width pulse. This is AND-gated with the SERIAL ONES from A3-8 by gate A1-8. (External bits may be inserted on this same line through pin 22.) The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A2-3 and A9-8 are used to combine the various widths to produce the output code at pin B.



CODE GENERATOR ASSEMBLY #021554-4-1 REV E

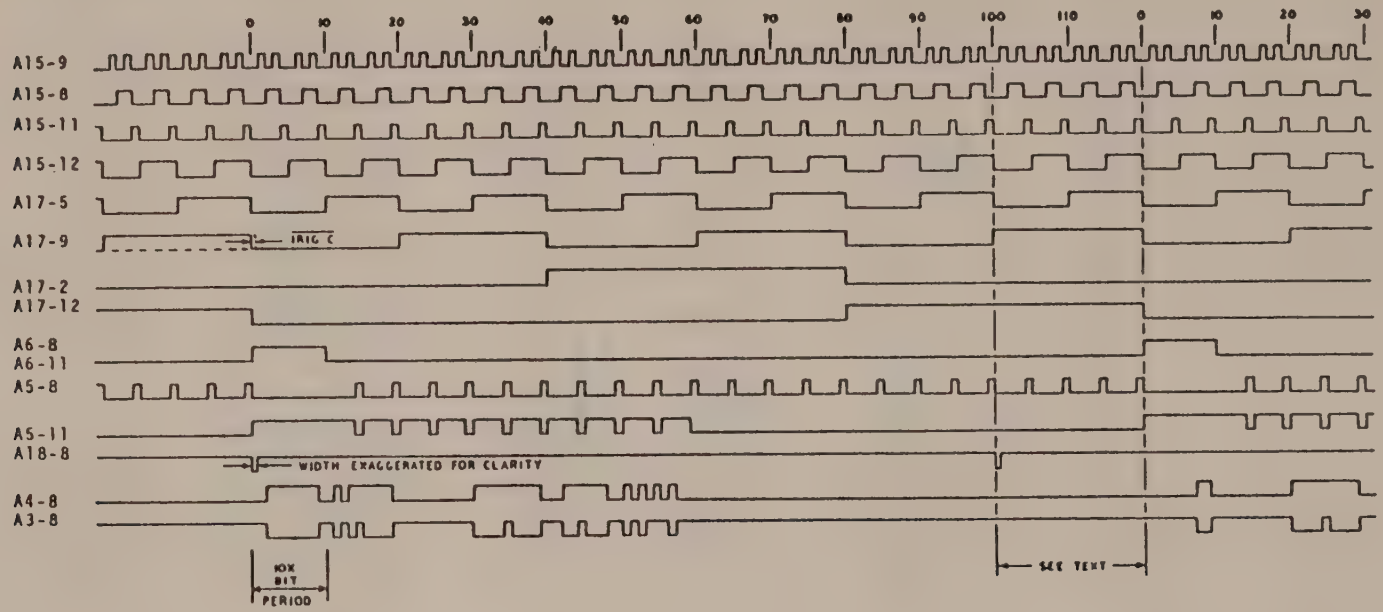
PARTS LIST
CODE GENERATOR #021554-7-1 REV E

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021554-4-1
	Schematic	021554-7-1
A1,2,5,6	Integrated Ckt, MC1810P	025735
A3,9	Integrated Ckt, MC846P	019716
A4,10-14	Integrated Ckt, 74151	02577101
A7,8,15	Integrated Ckt, 7490	025732
A16	Integrated Ckt, 74LS04	103749
A17	Integrated Ckt, 74LS197	103165
A18	Integrated Ckt, 7410	019706
C1	Capacitor, 39 µF, 10V	100183
C2	Capacitor, .001 µF	100076
C3	Capacitor, 100 pF, DM15	100173
L1	Inductor, R45-4	101313
R1	Resistor, 390Ω ¼w 5%	101592
R2-4	Resistor, 10K ¼w 5%	101570
W1	Jumper, Molded	102879
	Extractor	100865



NOTE
CODE SHOWN IS ARBITRARY AND
NOT NECESSARILY REALIZABLE.

IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 1 of 2)



NOTE:
CODE SHOWN (SERIAL ONES & A18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 2 of 2)

CIRCUIT DESCRIPTION

TIME-OF-DAY ACCUMULATOR

SCHEMATIC #021543-7-3

1) GENERAL

This card successively divides the 1 pps signal to provide outputs which represent seconds through hours. All outputs are buffered, an input inhibit circuit is provided, and the dividers are recycled to zero one second after reaching 23:59:59.

2) DIVIDERS

Dividers U1, U4, U7 and U8 are divide-by-10 circuits. Dividers U3 and U5 are divide-by-8 circuits. Recycle circuits formed from gates on U13 and U17 convert U1, U3 to a scale of 60, U7, U8 to a scale of 60 and U7, U8 to a scale of 24. Each divider has its data inputs, connected to a preset time source. Grounding the appropriate preset line will load the preset time into divider. Grounding pin 23 resets the Accumulator through gates on U9, U13 and U17.

3) RECYCLE CIRCUITS

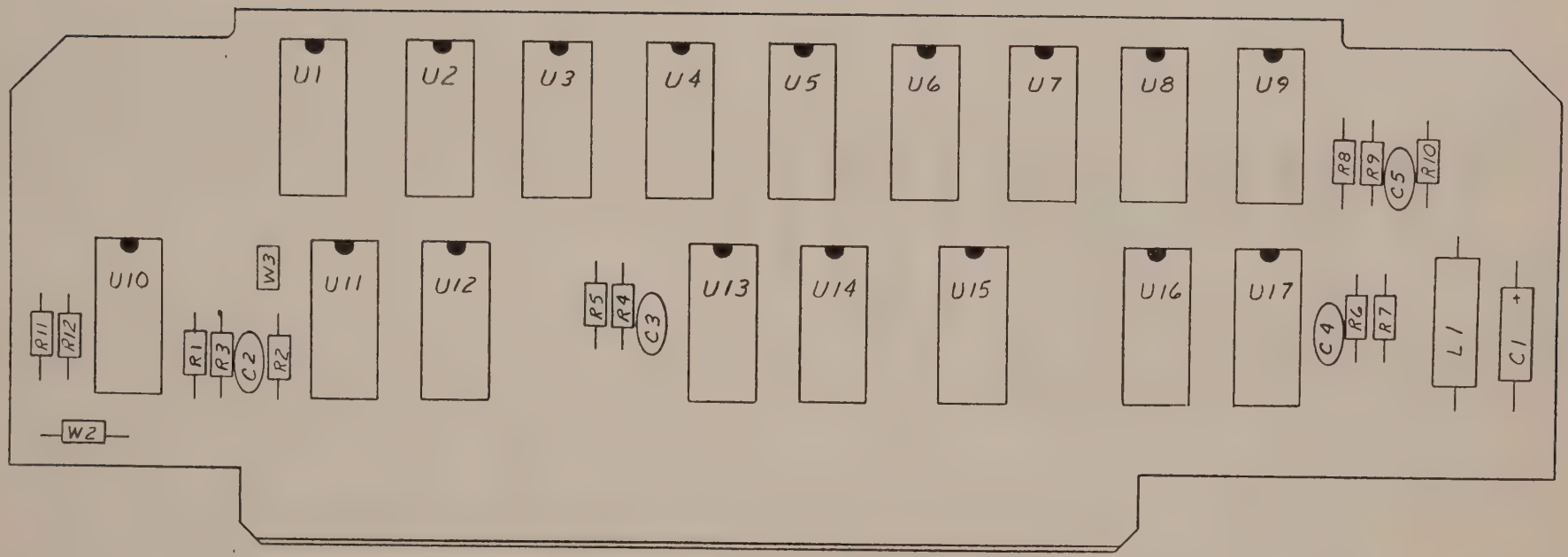
The scale of 60 recycle circuits for seconds and minutes are identical. The seconds circuit consists of AND gate U13-9 and a differentiating circuit formed from C3, R4 and R5. Gate U13-9 output goes high when U3 reaches a count of 5. It resets U1 and U3 through C3 and U13-6 when it returns low at the next count.

The scale of 24 recycle circuit for hours consists of AND gates U13-8, U17-8 and a differentiating circuit formed from C5, R9 and R10. The output from U17-8 goes high when U7 and U8 reach a count of 23. It resets U7 and U8 through C5 and U9-8,6 in tandem when it returns low at the next count.

4) INHIBIT CIRCUIT

The inhibit circuit is used to stop updating of the accumulator when the unit is in HOLD. Gate U10-6 inverts the $\overline{\text{1pps}}$ input. Gates U10-8,11 form an RS flip-flop. Gate U10-3 inverts the $\overline{\text{INHIBIT}}$/ENABLE line, pin A. When this line is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$/ENABLE input.

Programming jumper W3 is installed in the "A" position in Readers and Reader/Generators to prevent update of minutes and hours in reverse read operation. It is installed in the "B" position in Clocks and Generators where the ENABLE input to Pin A is used for $\overline{\text{HOLD}}$.



TOD ACCUMULATOR ASSEMBLY #021543-4-3 REV E

PARTS LIST
TIME-OF-DAY ACCUMULATOR #021543-7-3 REV E

REF.	DESCRIPTION	SD PART NO.
	Assembly	021543-4-3
	Schematic	021543-7-3
C1	Capacitor, 39 µF	100183
C2	Capacitor, 220 pF	117633
C3,4,5	Capacitor, 1000 pf	117639
R1,4,6,9	Resistor, 8.2K ¼w 5%	10159501
R2,5,7,8,10,11,12	Resistor, 10K ¼w 5%	10157001
R3	Resistor, 3.9K ¼w 5%	10160101
U1,4,7,8	Integrated Ckt, 74LS196	103164
U2,6	10K Resistor Pack	117241
U3,5	Integrated Ckt, 74LS197	103165
U9	Integrated Ckt, 74LS132	116946
U10	Integrated Ckt, 846	019716
U11 - U17	Integrated Ckt, 7408	103093
L1	Inductor, R45-4	101313
W2	Molded Jumper	102879
W3	Shorting Jack Mod.	08126101
	Shorting Jack	116979
	Pin, Swage	116978
	Extractor	100865

GENERAL DESCRIPTION
SHAPER AND MODULATOR PCB
SCHEMATIC #7-021556

1. GENERAL

The shaper and modulator pcb can be assembled to provide up to three shaper circuits, a modulator, a dc code output buffer, a days/ID control circuit, a square wave decoder and miscellaneous inverters and buffers. The shaper circuits are identical with the exception that three capacitors within each circuit are a function of frequency. The following description is intended to apply to all pcb configurations. The specific assembly used is covered by the attached assembly, schematic and parts list.

2. SHAPERS

Each of the shaper circuits (up to three) are identical, with the exception that the values chosen for three capacitors in each circuit are inversely proportional to the resonant frequency. Each shaper accepts a logic level squarewave at the selected carrier frequency and outputs an in-phase sine wave which may be selected (through switching external to the card) and fed to the modulator. The input is filtered and applied to the base of a constant-current amplifier which drives an active circuit having the electrical properties of a tuned tank circuit. A potentiometer is provided to adjust the resonant frequency. The sine wave output from the circuit is buffered and ac-coupled to output pin M, S or T.

3. MODULATOR

The modulator accepts the selected carrier sine wave at pin W and modulates it with the dc level shift code at pin F. The resulting modulated code is fed through amplifier A4 to output pin X.

A MODULATION RATIO adjustment, R16, sets the percentage of modulation before the signal is fed to A4. A MODULATED CODE AMPLITUDE adjustment, R20, determines the gain of amplifier A4, thus establishing the signal level at pin X (0 to ± 10 V p-p).

4. DC CODE BUFFER

The dc level shift code input to pin F is inverted once by A1-11 and again by Q4 before being fed as the dc code output to pin 21, through R25. Transistors Q2 and Q3, and the DC Code amplitude potentiometer R23 establish the output level at pin 21 (0.4 V to $+10$ V). Short circuit protection is provided by CR3, CR4 and R24. The quiescent current in Q3 and Q4 is determined by CR3, CR5 and R25.

5. DAYS/ID (RUN NUMBER(CONTROL

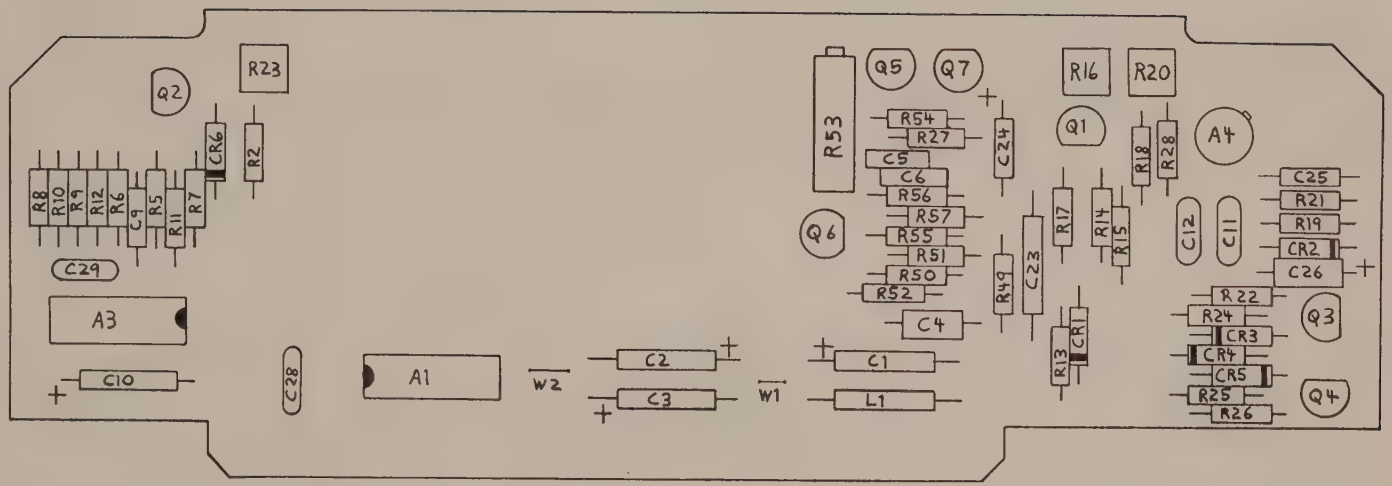
Gates on A3 conrol the selection of the signal which is used to update the days accumulator in the system. The carry output from the time-of-day accumulator is inverted and applied to A3-9. If the other input (the ID NUM line) is high (i.e., left open), the hours accumulator carry will update the days accumulator. Similarly, a high on the DAYS line permits a signal on pin B (ID NUM ADV) to update the days accumulator. The ID advance input pulses are standardized by one-shot A3-3, 6 to ensure relaible operation.

6. SQUARE WAVE DECODER

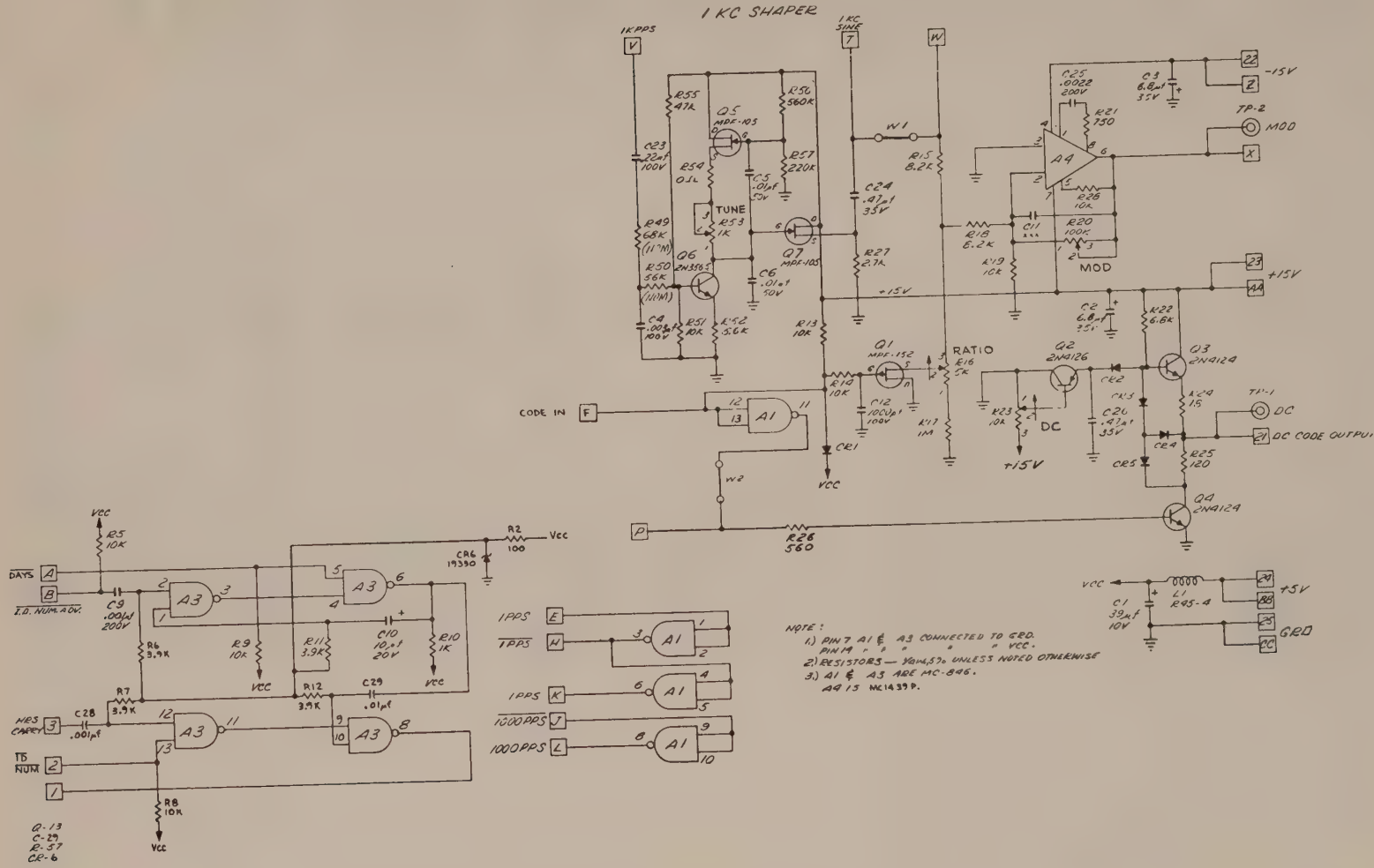
This circuit, formed from gates on A2, generates a square wave from the bcd outputs fed to pins C, D and N from an external decade counter. It consists of a flip-flop (A2-8, 11) which is ac-set at mid-period when the output from A2-6 goes to ground (1 and 4 of the 8-bit. The result is a square wave at A2-11. The output pulse rate is a function of the source of input signals.

7. BUFFERS

Extra gates on A1 and A2 are made available for external use as inverters and buffers.



SHAPER & MODULATOR ASSEMBLY #021556-7-5 REV D_2



SHAPER & MODULATOR SCHEMATIC #021556-7-5 REV E

PARTS LIST

SHAPER & MODULATOR #021556-7-5 REV H_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021556-4-5
	Schematic	021556-7-5
A1-3	Integrated Circuit, MC846P	019710
A4	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 6.8 µF, 35 V	100182
C4	Capacitor, .0033 µF, 200 V	100153
C5,6	Capacitor, .01 µF, 50 V	100132
C9	Capacitor, .001 µF, 200 V	100137
C10	Capacitor, 10 µF, 20 V	100063
C11	Capacitor, Factory Selected	XXXXXX
C12	Capacitor, 1000 pF, 100 V	100243
C23	Capacitor, .22 µF, 100 V	100148
C24,26	Capacitor, .47 µF, 35 V	100140
C25	Capacitor, .0022 µF, 200 V	100185
C28	Capacitor, 1000 pF Disc	100076
C29	Capacitor, .01 µF, Disc	100103
CR1-5	Diode, 1N4151	100385
CR6	Diode, 19330	019330
L1	Inductor, R45-4	101313
Q1	Transistor, MPF-152	101383
Q2	Transistor, 2N3906	101378
Q3,4	Transistor, 2N3904	101377
Q5,7	Transistor, MPF-105	101384
Q6	Transistor, 2N3565	101371
R2	Resistor, 100 Ω 5%, 1/4 W, CC	101609
R5,8,9,13,14, 19,28,51	Resistor, 10 k 5%, 1/4 W, CC	101570
R6,7,11,12	Resistor, 3.9 k 5%, 1/4 W, CC	101601
R10	Resistor, 1 k 5%, 1/4 W, CC	101569
R15,18	Resistor, 8.2 k 5%, 1/4 W, CC	101595
R16	Resistor, 5 k 62 PA, Var.	101845
R17	Resistor, 1 M 5%, 1/4 W, CC	101605
R20	Resistor, 100 k 62 PA, Var.	101934
R21	Resistor, 750 Ω 5%, 1/4 W, CC	101689
R22	Resistor, 6.8 k 5%, 1/4 W, CC	101544

PARTS LIST

SHAPER & MODULATOR #021556-7-5 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R23	Resistor, 10 k 62 PA, Var.	101937
R24	Resistor, 18 Ω 5%, 1/4 W, CC	101727
R25	Resistor, 120 Ω 5%, 1/4 W, CC	101717
R26	Resistor, 560 Ω 5%, 1/4 W, CC	101583
R27	Resistor, 2.7 k 5%, 1/4 W, CC	101599
R49	Resistor, 68 k 5%, 1/4 W, CC	101597
R50	Resistor, 56 k 5%, 1/4 W, CC	101670
R52	Resistor, 5.6 k 5%, 1/4 W, CC	101584
R53	Resistor, 1 k 79 P, Beckman, Var.	101181
R55	Resistor, 47 k 5%, 1/4 W, CC	101574
R56	Resistor, 560 k 5%, 1/4 W, CC	101687
R57	Resistor, 220 k 5%, 1/4 W, CC	101610
	Extractor	100867

CIRCUIT DESCRIPTION
MINOR COUNTER PCB
SCHEMATIC #021632-7-2

1. GENERAL

The Minor Counter card can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel bcd outputs. Provision is made to gate one set of bcd outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. Provision is included for three output pulse rates with 10% duty cycle which may be supplied in place of the days recycle circuit.

2. DECADE DIVIDERS

The up to three decade dividers are connected in tamdem. Each is provided with parallel bcd data inputs which may be used to load preset information when the associated data strobe (PRESET) line is grounded. Jumpers W1 and W2 permit the data strobe associated with the center decade (A4) to be wired in common with the data strobe input to the first decade (A1) or the third (A6). The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel bcd outputs from each decade are wired to output pins through two sets of buffers.

3. OUTPUT BUFFERS

The bcd output buffers may be inverting or noninverting. One of the two sets (A10, A13 and A15) can be gated by inputs through pin L, K and J, respectively. These gate lines are buffered by inverters on A11.

4. INPUT INHIBIT CIRCUIT

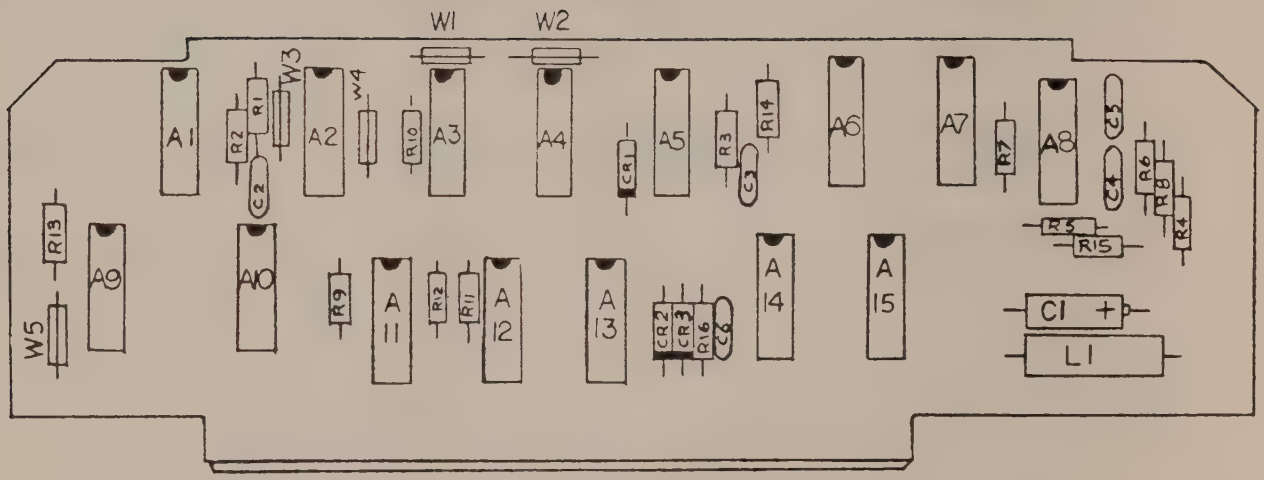
This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8, 11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5. OUTPUT PULSE RATES

Three sets of gates are used to produce three 10% duty cycle pulse rates. Each pulse goes high when the four outputs from the corresponding decades are low (leading edge on time). The pulse remains up until the output of the decade in 001. Thus, the pulse is high 10% of the time. The output is a 5 V logic level behind 6 kΩ.

The pulse rate outputs are fed to pins A, S and T which are used for units preset and days recycle inputs on other configurations of the card. Chip A5 is removed when the rate outputs are supplied.



DAYS ACCUMULATOR ASSEMBLY #021632-4-1 REV C

PARTS LIST

MINOR COUNTER #021632-7-2 REV E_1

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021632-4-1
	Schematic	021632-7-2
A1,4,6	Integrated Ckt, 74LS196	103164
A2,11	Integrated Ckt, MC846P	019716
A3,7	Integrated Ckt, MC1810P	025735
A8	Integrated Ckt, 7400	019705
A9,12,14	Integrated Ckt, MC1806P	025733
A10,13,15	Integrated Ckt, MC1808P	025734
C1	Capacitor, 39 µF, 10V	100183
C2	Capacitor, 220 pF, DM	100220
L1	Inductor, R45-4	101313
R1	Resistor, 8.2K ¼w 5%	10159502
R2,9,10-15	Resistor, 10K ¼w 5%	10157002
R4	Resistor, 3.9K ¼w 5%	10160102
W1-W4	Jumper, Molded	102879

CIRCUIT DESCRIPTION
TIME BASE/SERIAL PRESET-RESET
SCHEMATIC #021566-7-15

1) GENERAL

This version of the Time Base/Serial Preset-Reset Card contains only the basic Time Base and Divider circuits.

2) TIME BASE

The Time Base section consists of an unheated crystal, Y1, and feedback amplifier Q1. Ths oscillator output, at pin Y, may be utilized as an external reference or it bay be jumpered to pin W for internal use on the card. An external reference signal may be utilized by applying it to pin W in place of the above signal.

The time base signal is applied to the base of voltage-amplifier Q2 (which has a gain of three), isolated, and applied to the base of Q3. Clipper-circuit Q3 provides a 5 V p-p square wave at pin X.

3) DIVIDER CHAIN

Control gate A5-6 receives the output of Q3 (jumper W1 installed) or an input through pin 13 depending upon the time base pulse rate and the application.

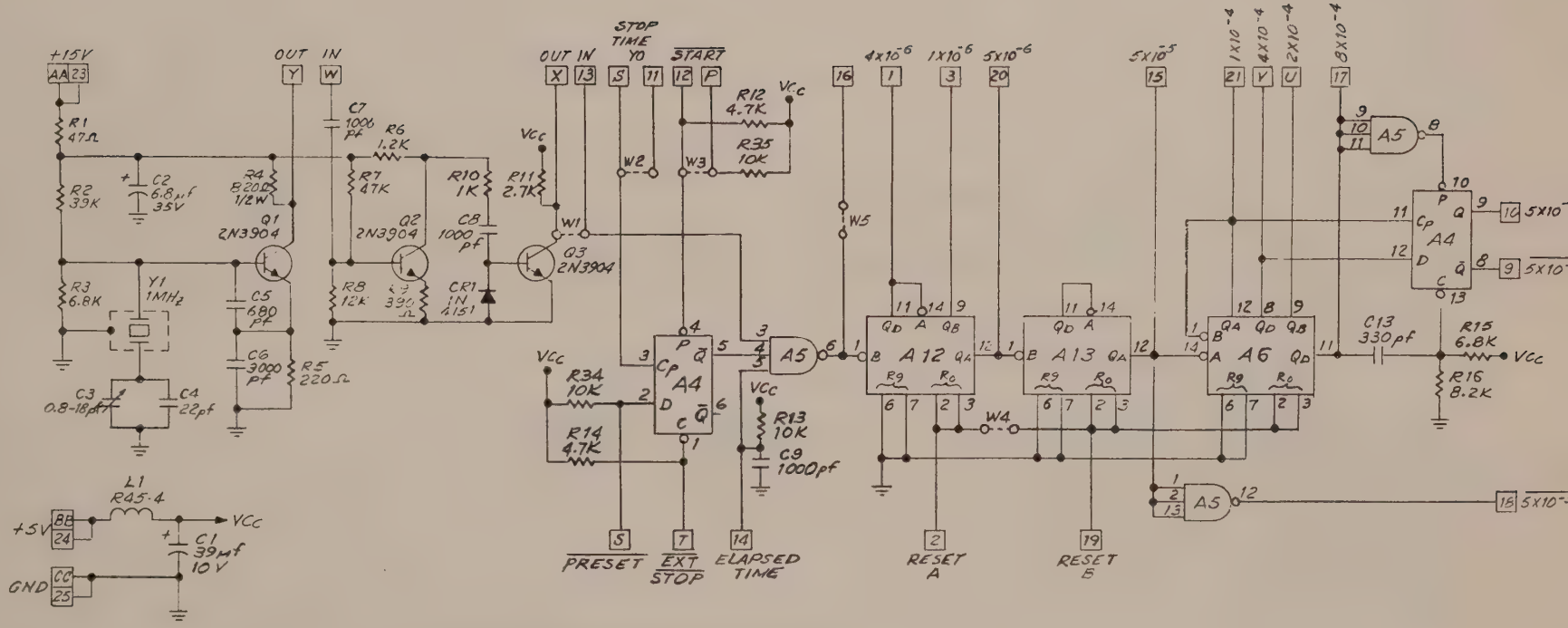
The time base pulse rate at this point is usually 1 Mpps. Control gate A5-6 has two other inputs. One is the Elapsed Time input from pin 14 and the other is from Stop/Start flip-flop A4-5.

When a Logic 0 (ground) is applied to the External Stop line (pin T), flip-flop A4-3 will generate a Logic 0 which will close gate A5-6 and inhibit the time base input to the divider chain. A positive transition on pin 11 or R, (the Stop time input) will also inhibit the time base if pin S is at ground.

A ground signal on the $\overline{\text{START}}$ pin 12 or P, will clear the inhibit from A5-6.

The divider chain consists of up to three divider chips (A12, A13 and A6) connected in tandum. In most card configuration, these are used as decades. They divide the 1 Mpps time base down to 1 Kpps. The first two (A12 and A13) are connected as divide-by-5, then-by-2 counters. These develope 100 Kpps and 10 Kpps square waves at pin 20 and 15, respectively. The third decade (A6) is connected in the normal divide-by-2, then-by-5 arrangement. BCD outputs (1-2-4-8) are provided at pins 21, U, V and 17. Flip-flop A4-9 developes complementary 1 Kpps square wave outputs at pins 10 and 9.

Pin 2 is the zero reset input to A12. The zero reset input to A13 and A6 are connected to pin 19. These two inputs may be jumpered together through W4. These lines must be grounded if not in use.

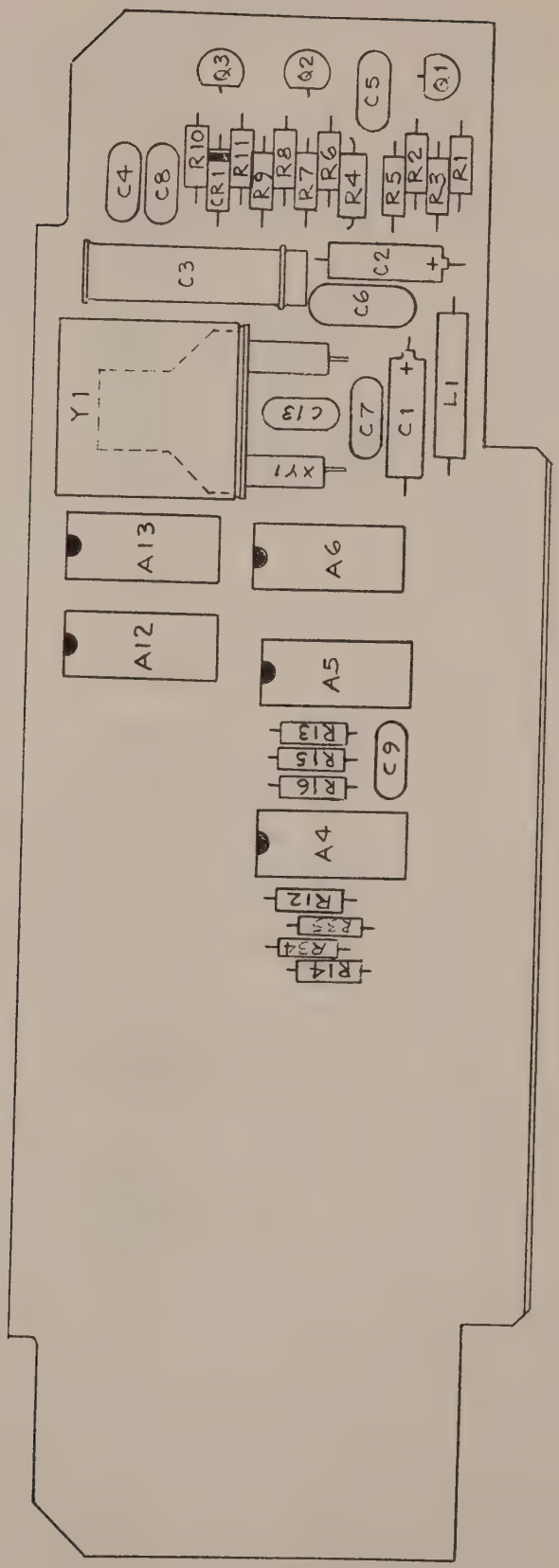


NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 1/4 W CARB COMP VALUED IN OHMS @ 5%
2. INT CKTS ARE AS FOLLOWS;

REF	JEDEC N2	TYPE	Vcc	GND
A4	SN7474N	DUAL D FLIP FLOP	14	7
A5	SN7410N	TRI (3 INPUT) NAND GATE	14	7
A6,12,13	SN7490N	DECADE COUNTER	5	10

TIME BASE SCHEMATIC #021566-7-15 REV A

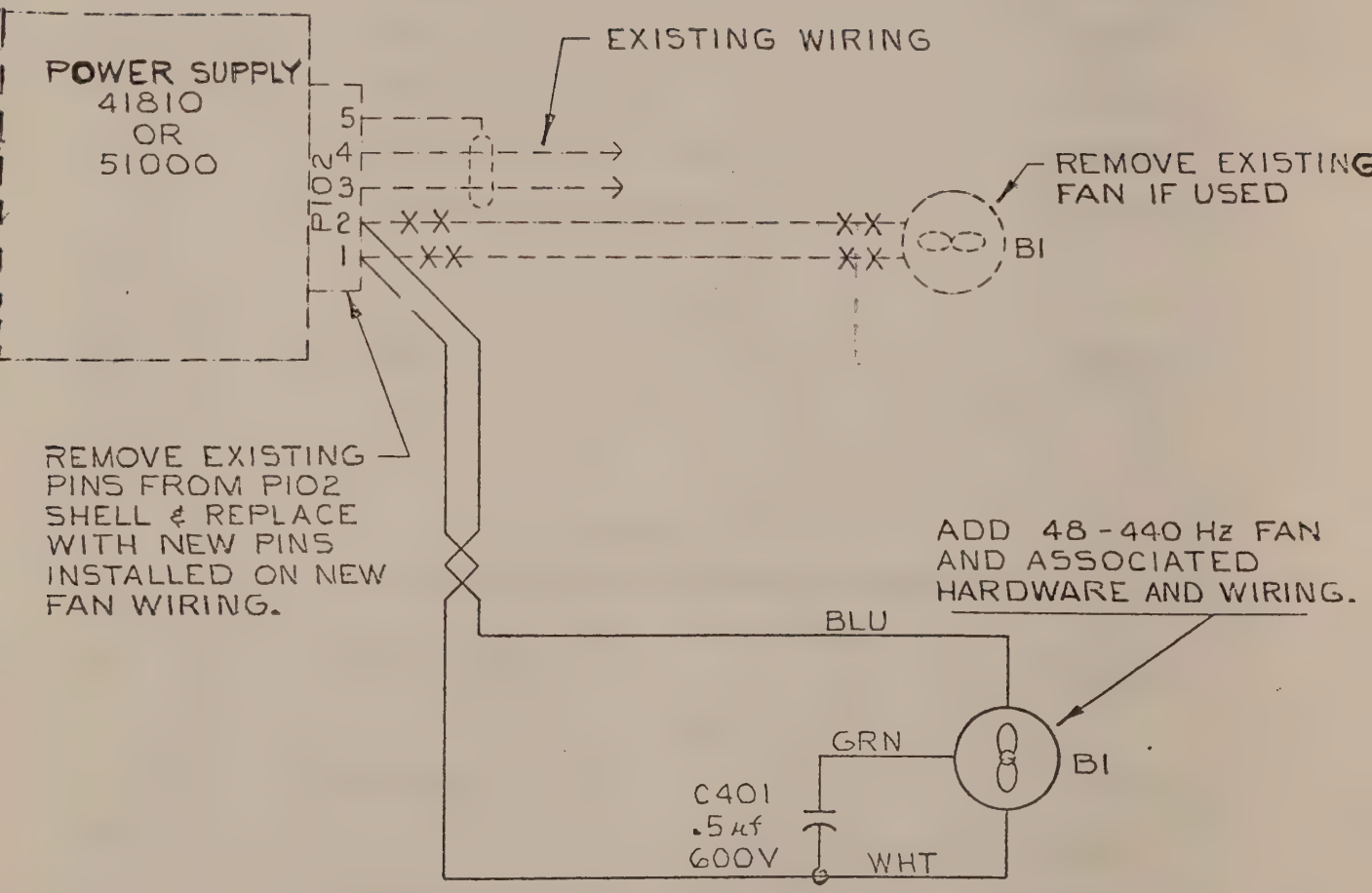


TIME BASE ASSEMBLY #021566-4-15

PARTS LIST

TIME BASE #021566-7-15 REV A_1

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021566-4-15
	Schematic	021566-7-15
A4	Integrated Ckt, 7474	025241
A5	Integrated Ckt, 7410	019706
A6,12,13	Integrated Ckt, 7490	025732
C1	Capacitor, 39µF 10V	100183
C2	Capacitor, 6.8µF 35V	100182
C3	Capacitor, 0.8-18pF	100102
C4	Capacitor, 22pF 100V	1176410
C5	Capacitor, 680pF 100V	1176380
C6	Capacitor, 3000pF 500V	100149
C7,8,9	Capacitor, 1000pF 100V	1176390
C13	Capacitor, 330pF	1176360
CR1	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1-3	Transistor, 2N3904	101377
R1	Resistor, 47Ω ¼w 5%	1015600
R2	Resistor, 39K ¼w 5%	1015610
R3,15	Resistor, 6.8K ¼w 5%	1015440
R4	Resistor, 820Ω ½w 5%	101656
R5	Resistor, 220Ω ¼w 5%	1015660
R6	Resistor, 1.2K ¼w 5%	1015810
R7	Resistor, 47K ¼w 5%	1015740
R8	Resistor, 12K ¼w 5%	1015650
R9	Resistor, 390Ω ¼w 5%	1015920
R10	Resistor, 1K ¼w 5%	1015690
R11	Resistor, 2.7K ¼w 5%	1015990
R12,14	Resistor, 4.7K ¼w 5%	1015980
R13,34,35	Resistor, 10K ¼w 5%	1015700
R16	Resistor, 8.2K ¼w 5%	1015950
	Eyelet	100534
XY1	Crystal Socket	100769
Y1	Crystal, 1 MHz	102450
	Extractor	100865



SCHEMATIC #7-05183201 FAN 48-440 Hz

PARTS LIST
OPTION L12 48-440 Hz FAN #7-05183202

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-05183201
B1	Fan	100037
P102-1/-2	Connector, 18 pin	10282202
C401	Capacitor, .5 µF, 600 V	100353
	Bracket, Cap Mounting	05183402
	DELETE	
B1	Fan	100038

PARTS LIST
OPTION L12 48-440 Hz FAN #7-05183201 Rev

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-05183201
B1	Fan	100037
C401	Capacitor, .5 µF, 600 V	100353
	Bracket, Fan Mounting	05183402
	Guard, Fan	100886
	DELETE	
B1	Screen, Fan	051927

APPENDIX A
INTERFACE INFORMATION

A.1 GENERAL

This appendix contains drawings which provide interfacing between the Systron-Donner Tape Search Unit and various makes and model of magnetic tape transport units. Optional connections are shown by dotted lines. These drawings are considered accurate and up-to-date. However, because of changes and modifications performed on many of the magnetic tape transport units by their respective manufacturers, complete accuracy of all interface drawings may not always be possible. Therefore, these drawings should be used primarily as a guide.

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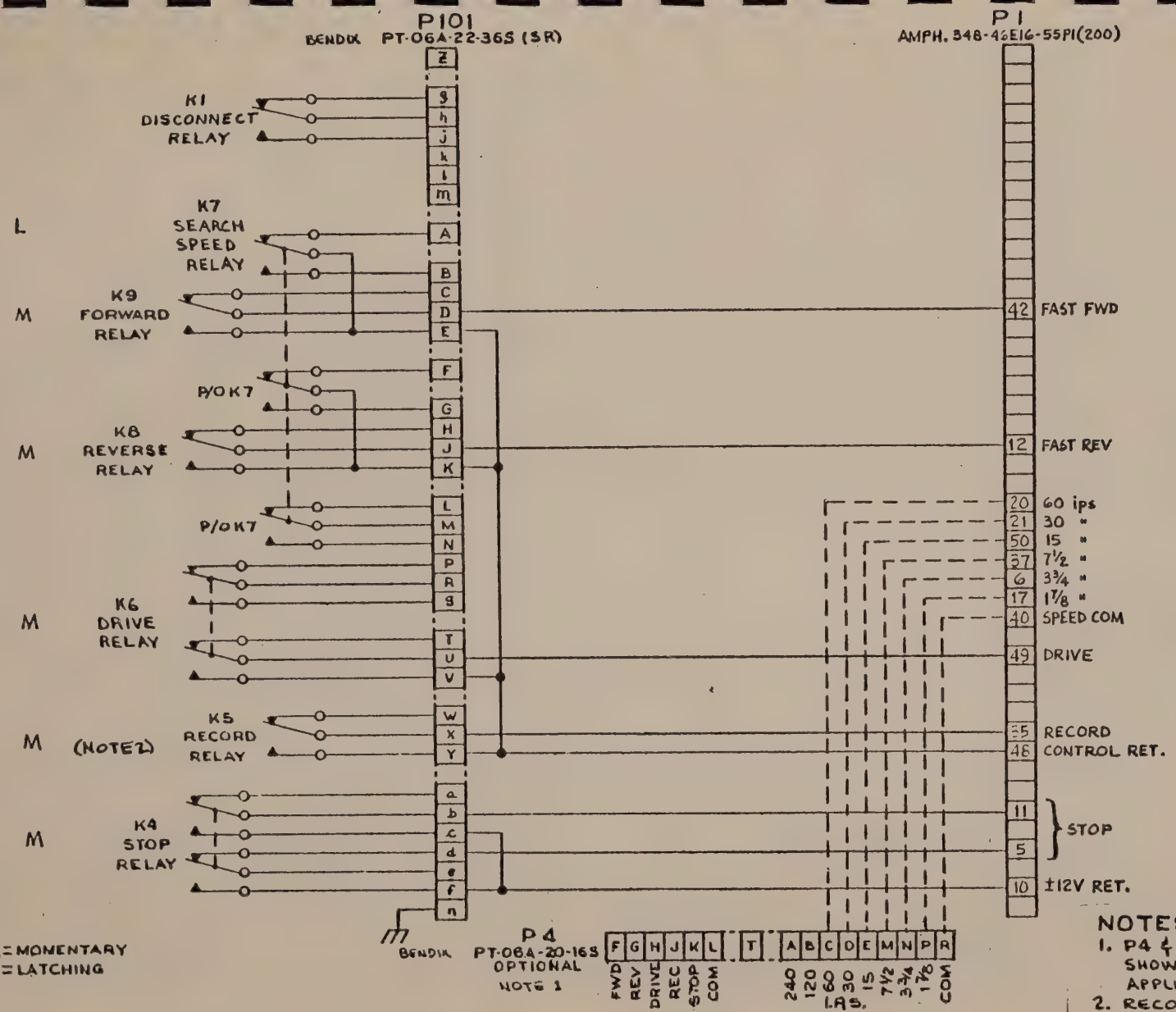
Sangamo 4700 Series	031528-7-1	A-48
Sangamo 4900 (Sabre IV)	041335-7-34	A-49
Sangamo (Sabre VI)	041335-7-93	A-50

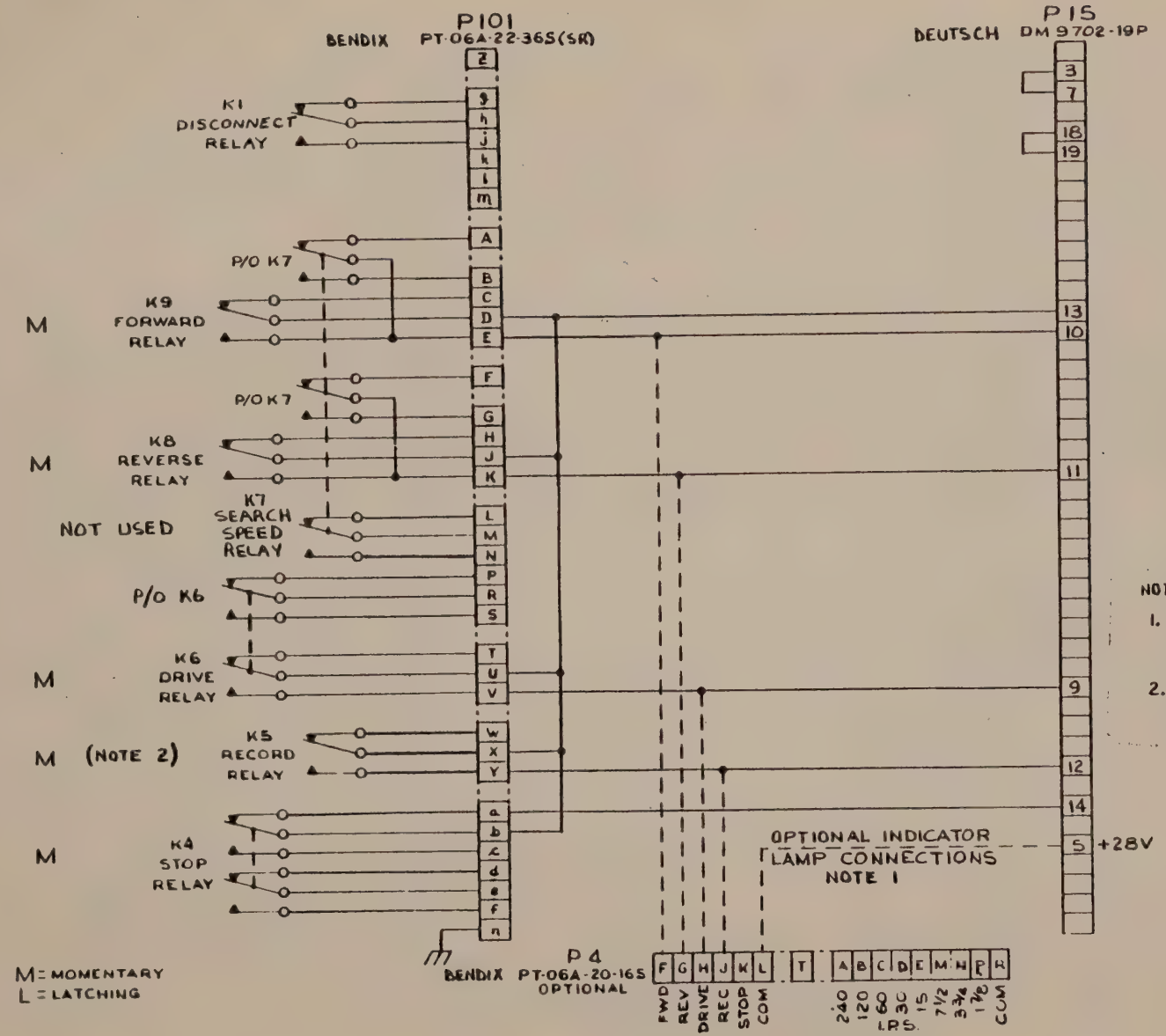
Note: Bendix Connector P101 mates with J101 on the Model 8140. On Models 8134 and 8154 it mates with J401.



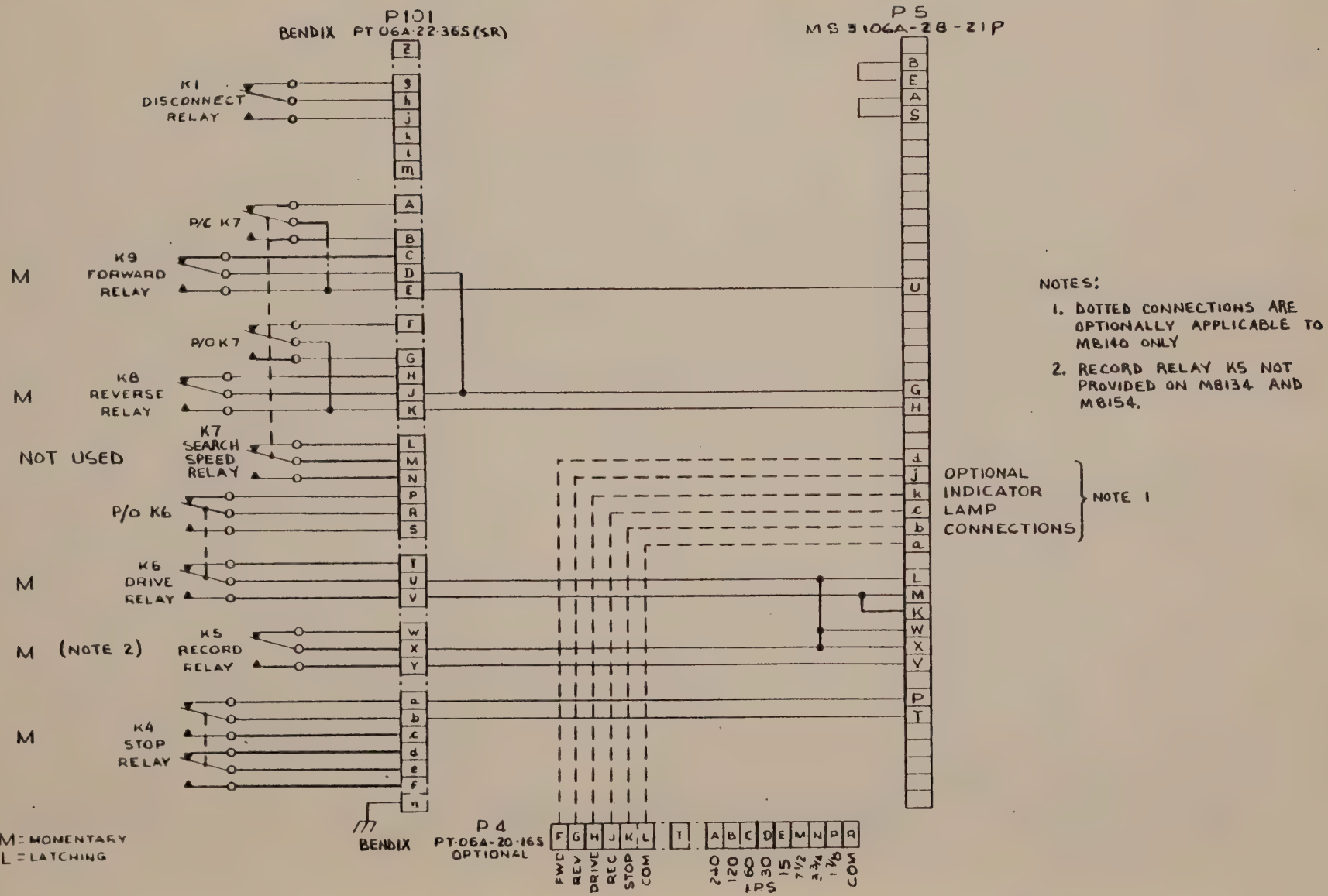
NOTES:

1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134
3. DRIVE FWD/REV SWITCH ON TRANSPORT MUST BE IN FWD POSITION.

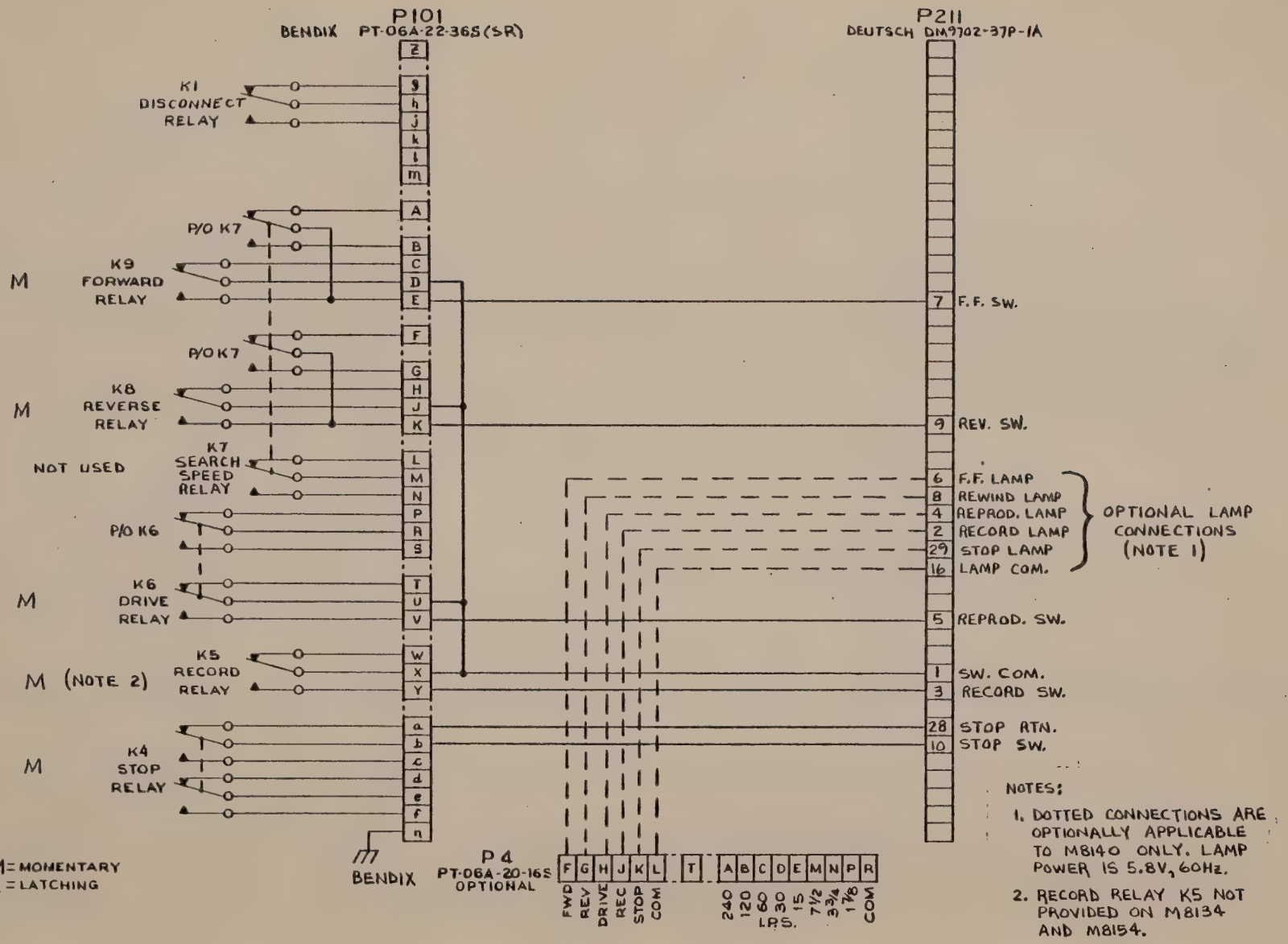
INTERFACE CABLE TO AMPEX AR-700 #041335-7-80 REV A



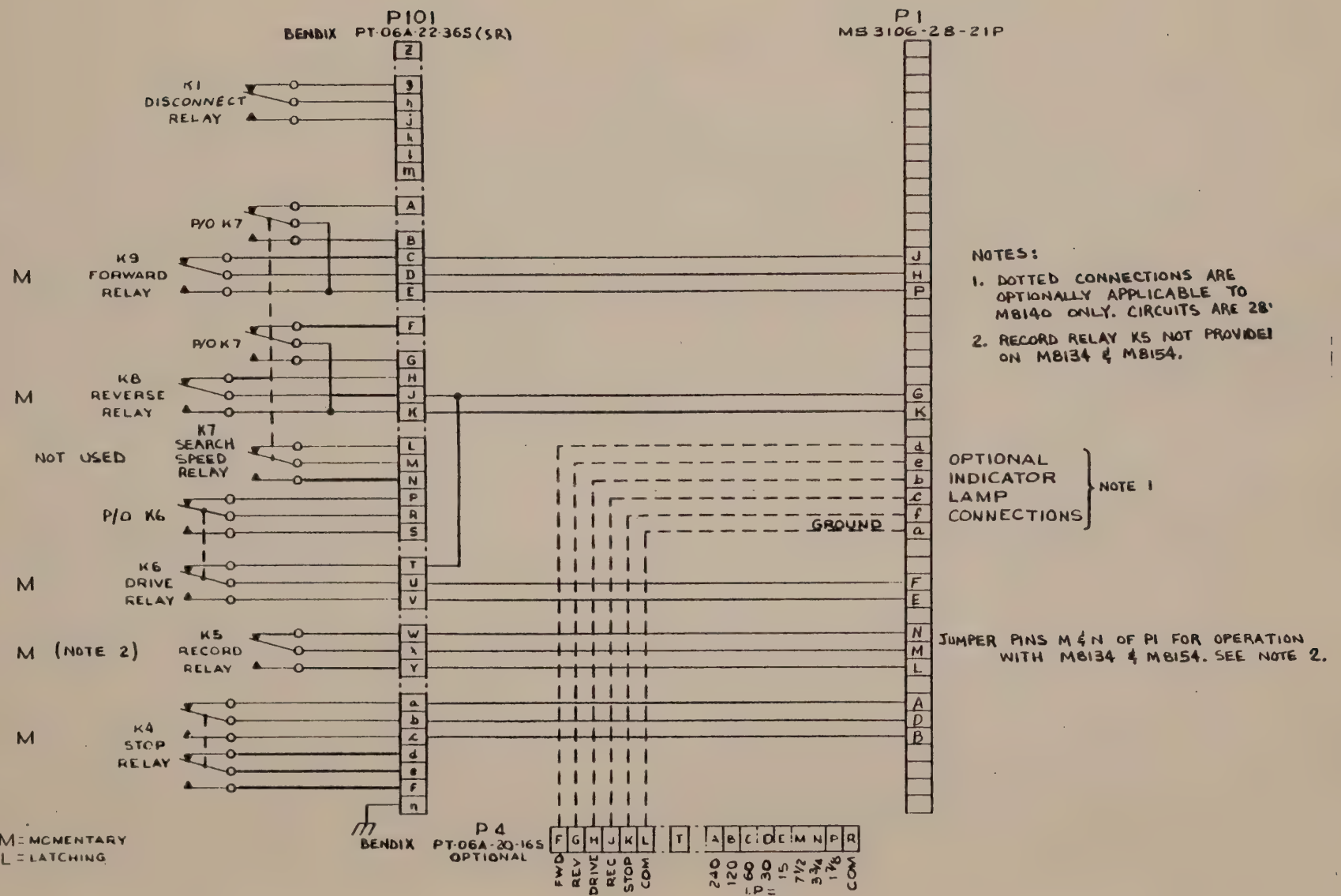
INTERFACE CABLE TO AMPEX CP100 #021941-7 REV C



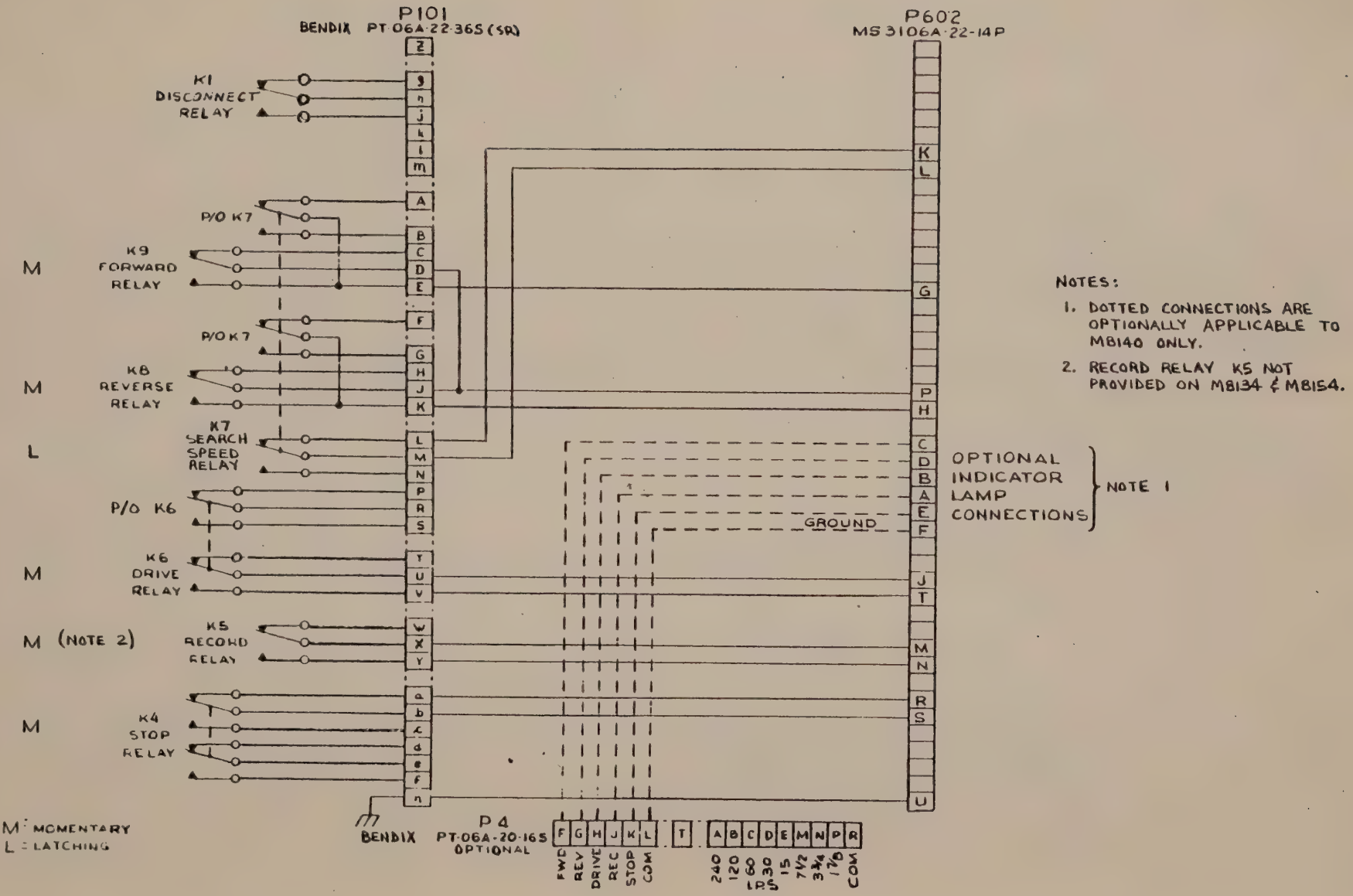
INTERFACE CABLE TO AMPEX FR100 #021943-7 REV C



INTERFACE CABLE TO AMPEX FR600/FR1400 #021979 REV C



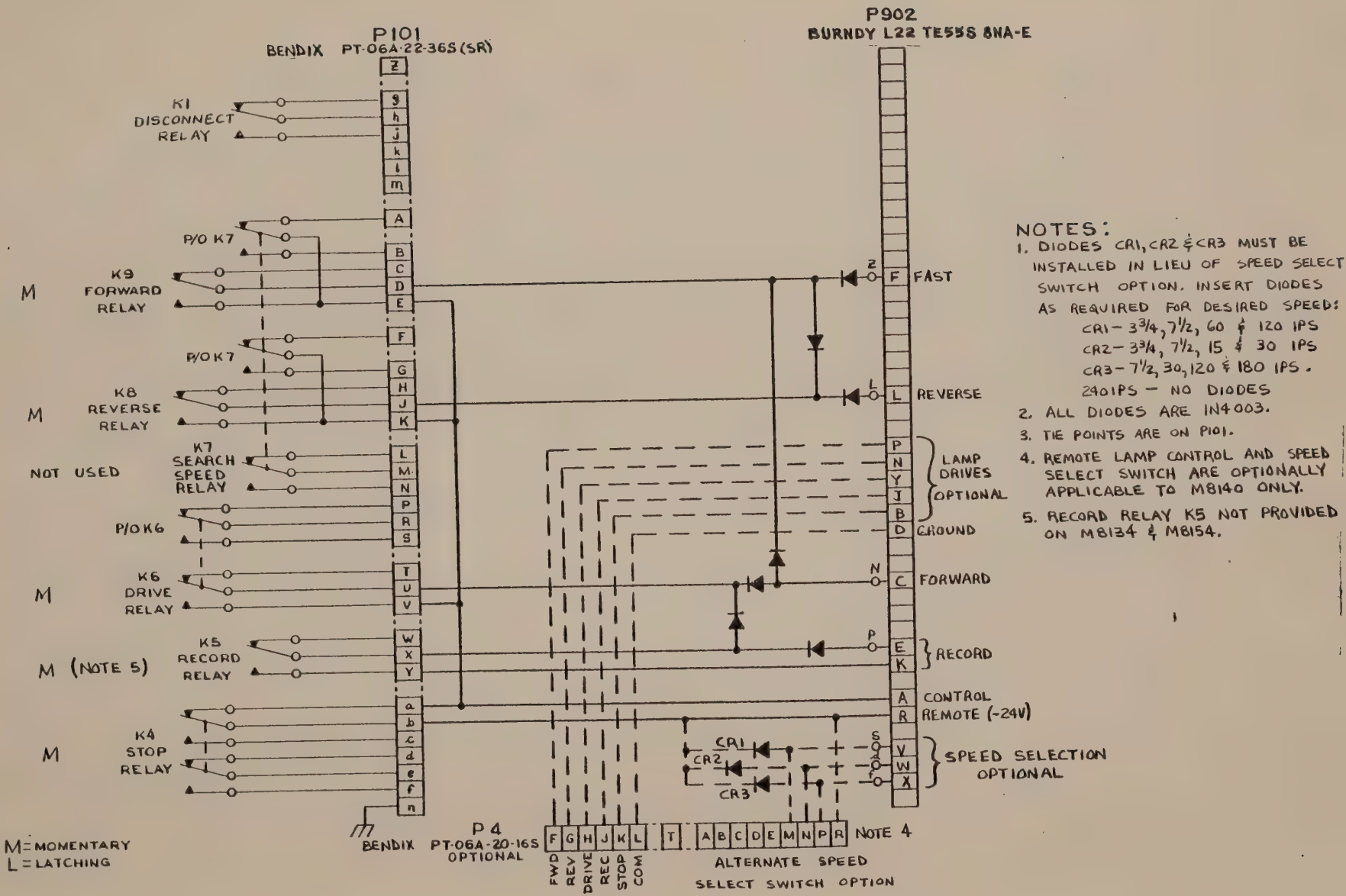
INTERFACE CABLE TO AMPEX FR1200 #021944-7 REV C



NOTES:

1. DOTTED CONNECTIONS ARE OPTIONALLY APPLICABLE TO M8140 ONLY.
2. RECORD RELAY K5 NOT PROVIDED ON M8134 & M8154.

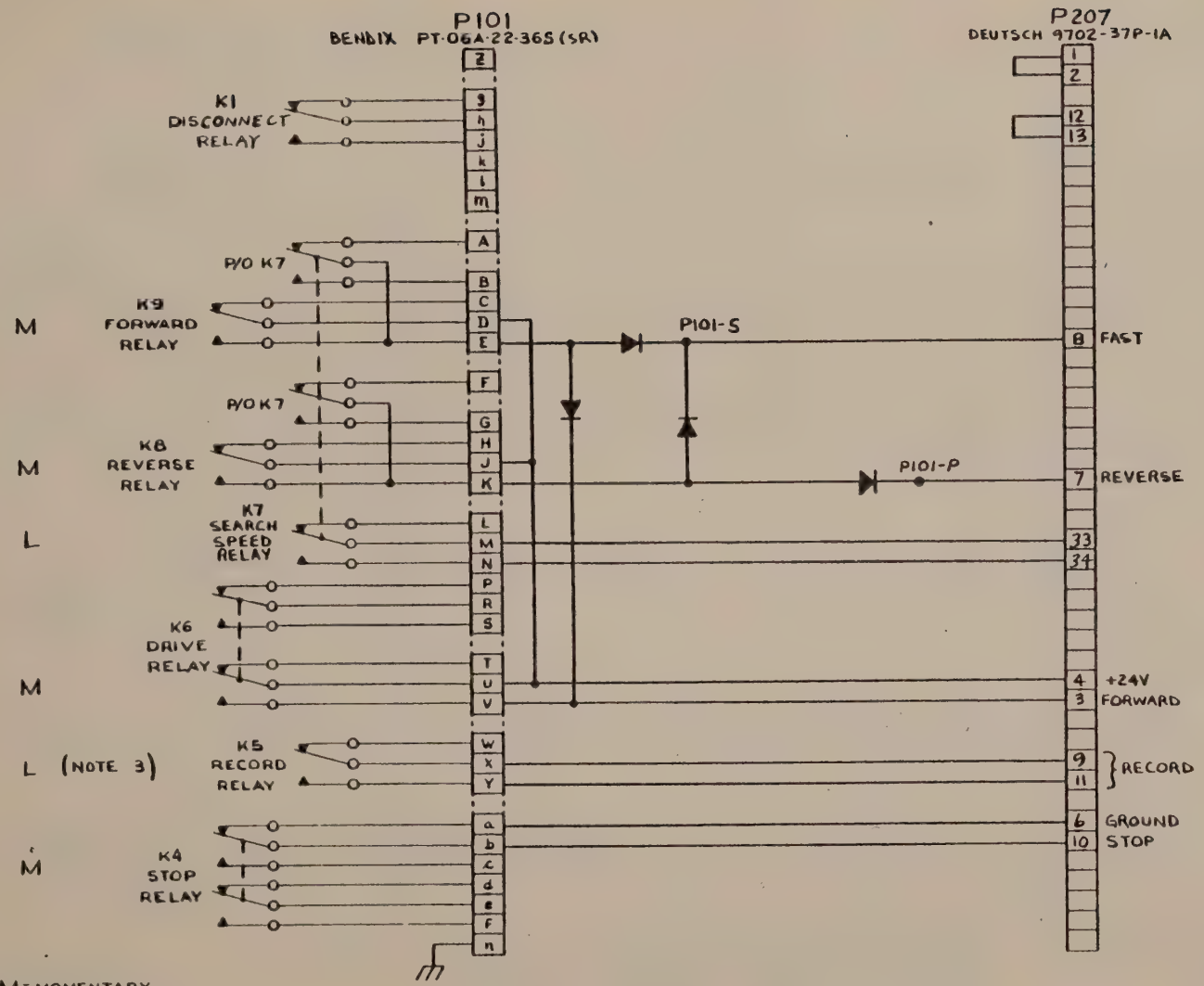
INTERFACE CABLE TO AMPEX FR1300 #021945-7 REV D



NOTES:

1. DIODES CR1, CR2 & CR3 MUST BE INSTALLED IN LIEU OF SPEED SELECT SWITCH OPTION. INSERT DIODES AS REQUIRED FOR DESIRED SPEED:
   CR1 – 3¾, 7½, 60 & 120 IPS
   CR2 – 3¾, 7½, 15 & 30 IPS
   CR3 – 7½, 30, 120 & 180 IPS.
   240 IPS – NO DIODES
2. ALL DIODES ARE IN4003.
3. TIE POINTS ARE ON P101.
4. REMOTE LAMP CONTROL AND SPEED SELECT SWITCH ARE OPTIONALLY APPLICABLE TO M8140 ONLY.
5. RECORD RELAY K5 NOT PROVIDED ON M8134 & M8154.

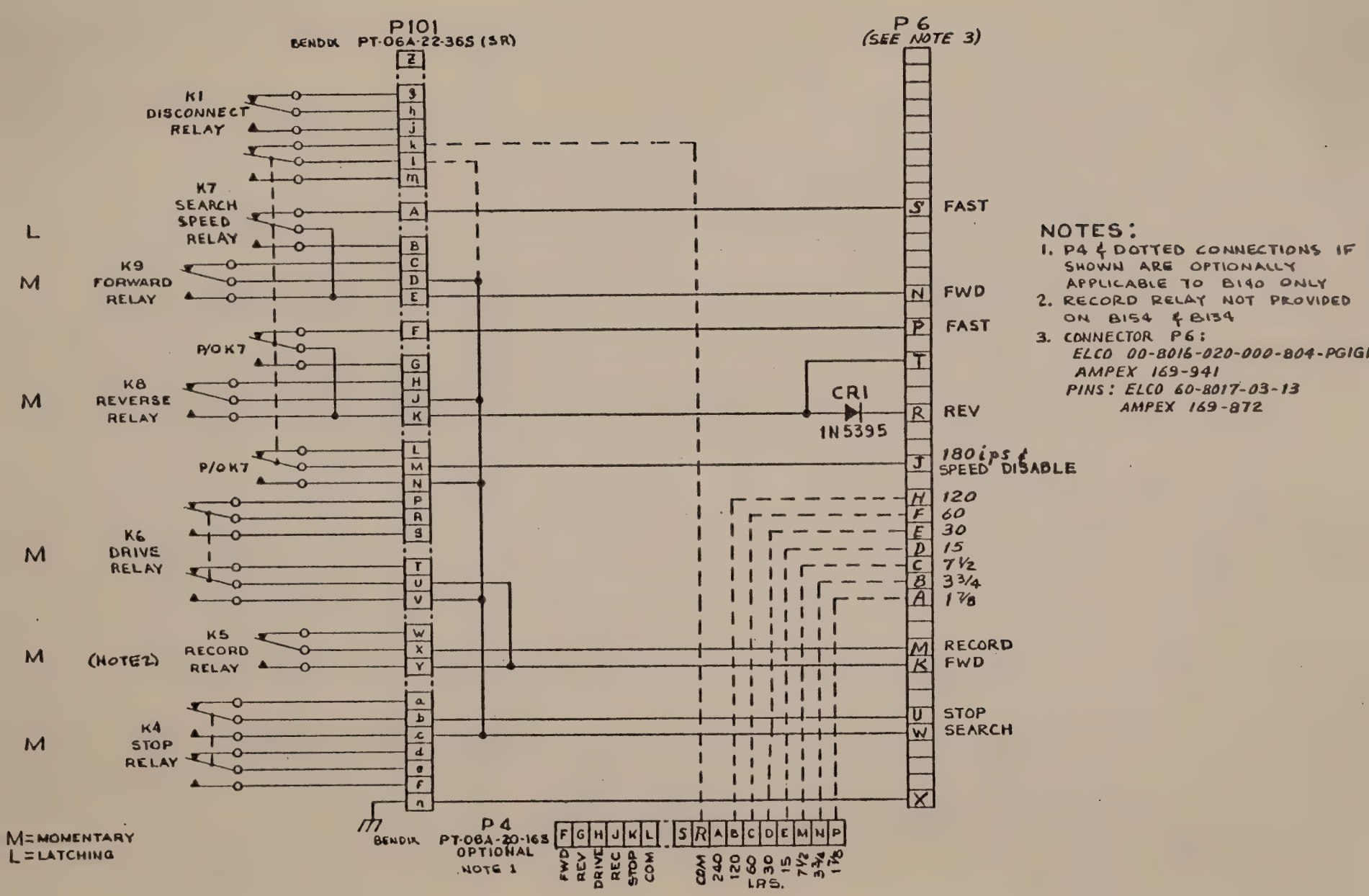
INTERFACE CABLE TO AMPEX FR1600/IV #021980-7 REV D



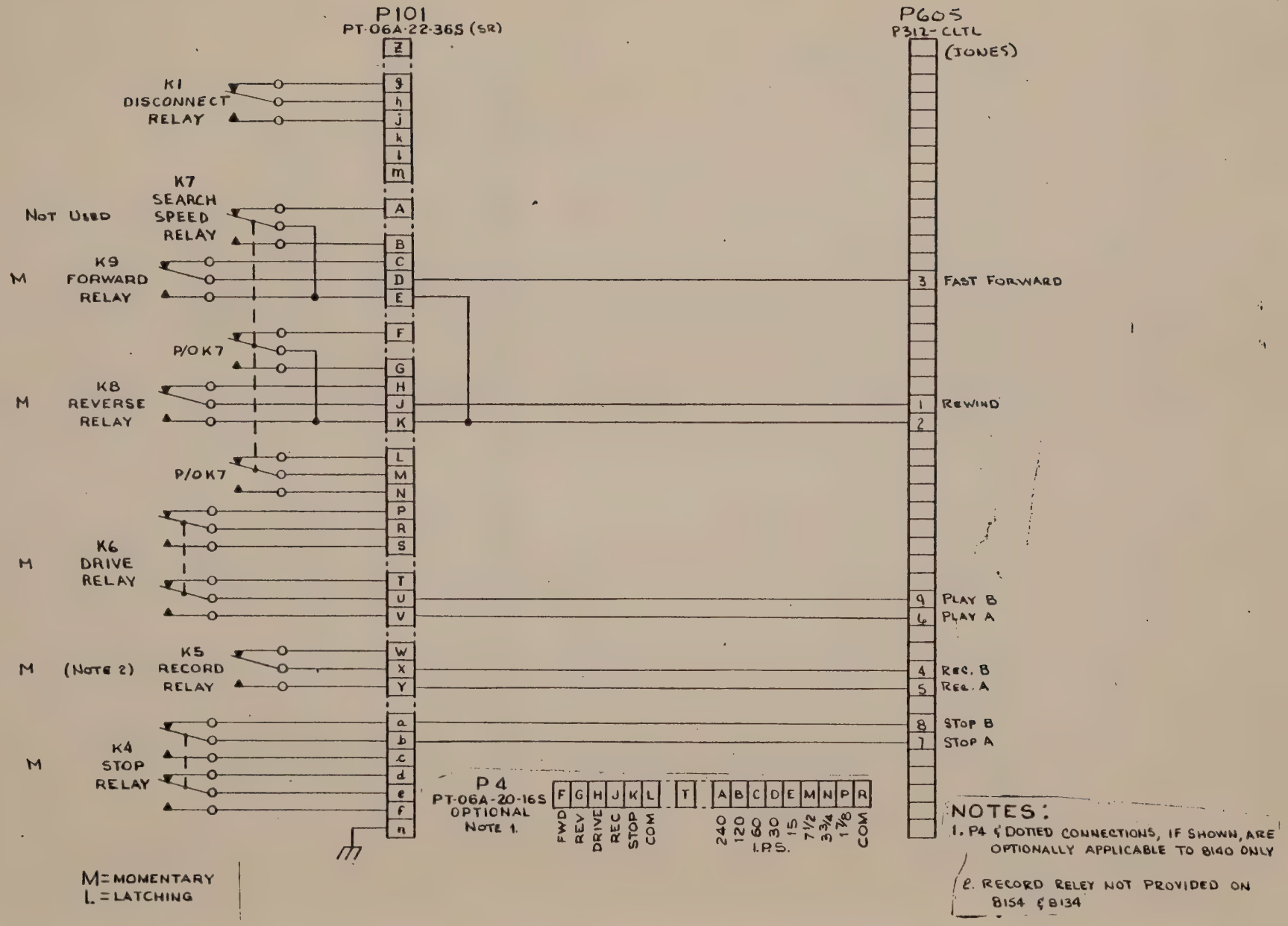
NOTES:

1. DIODES ARE IN4005
2. A FIELD MODIFICATION KIT IS REQUIRED TO ADAPT FR1800/FR1900 TRANSPORTS FOR TAPE SEARCH OPERATION.
   OLDER UNITS WITH -10 SYSTEM CONTROL BAY USE AMPEX PART Nº 1228091-01.
   NEWER UNITS WITH -11 SYSTEM CONTROL BAY USE AMPEX PART Nº 1228091-02.
   SEE REAR OF SYSTEM CONTROL BAY MODULE TO DETERMINE IF -10 OR -11.
3. RECORD RELAY K5 IS PROVIDED ON M8140 ONLY.

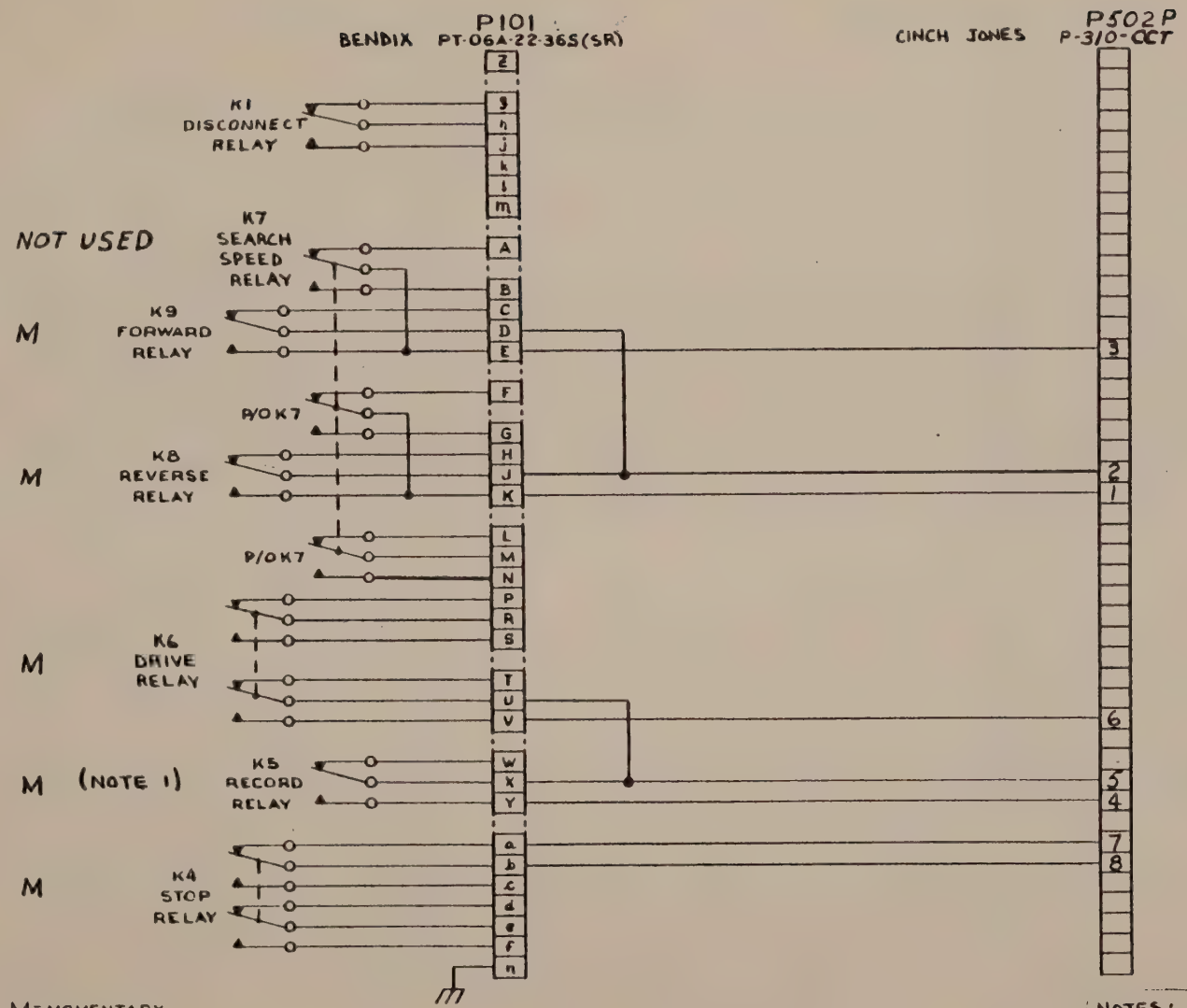
INTERFACE CABLE TO AMPEX FR1800/FR1900 #021956-7 REV C



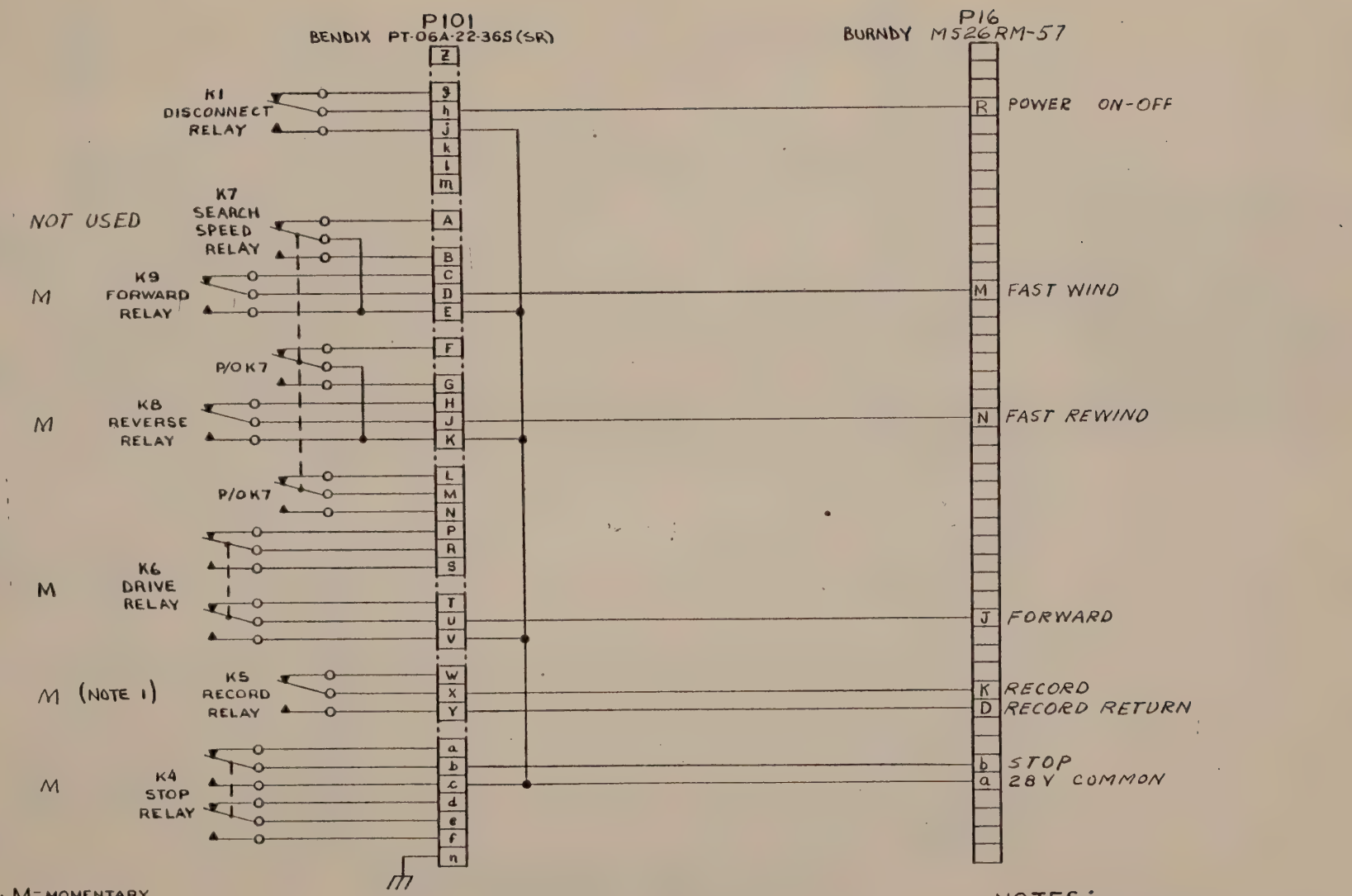
INTERFACE CABLE TO AMPEX FR2000/3000 #04149208 REV A



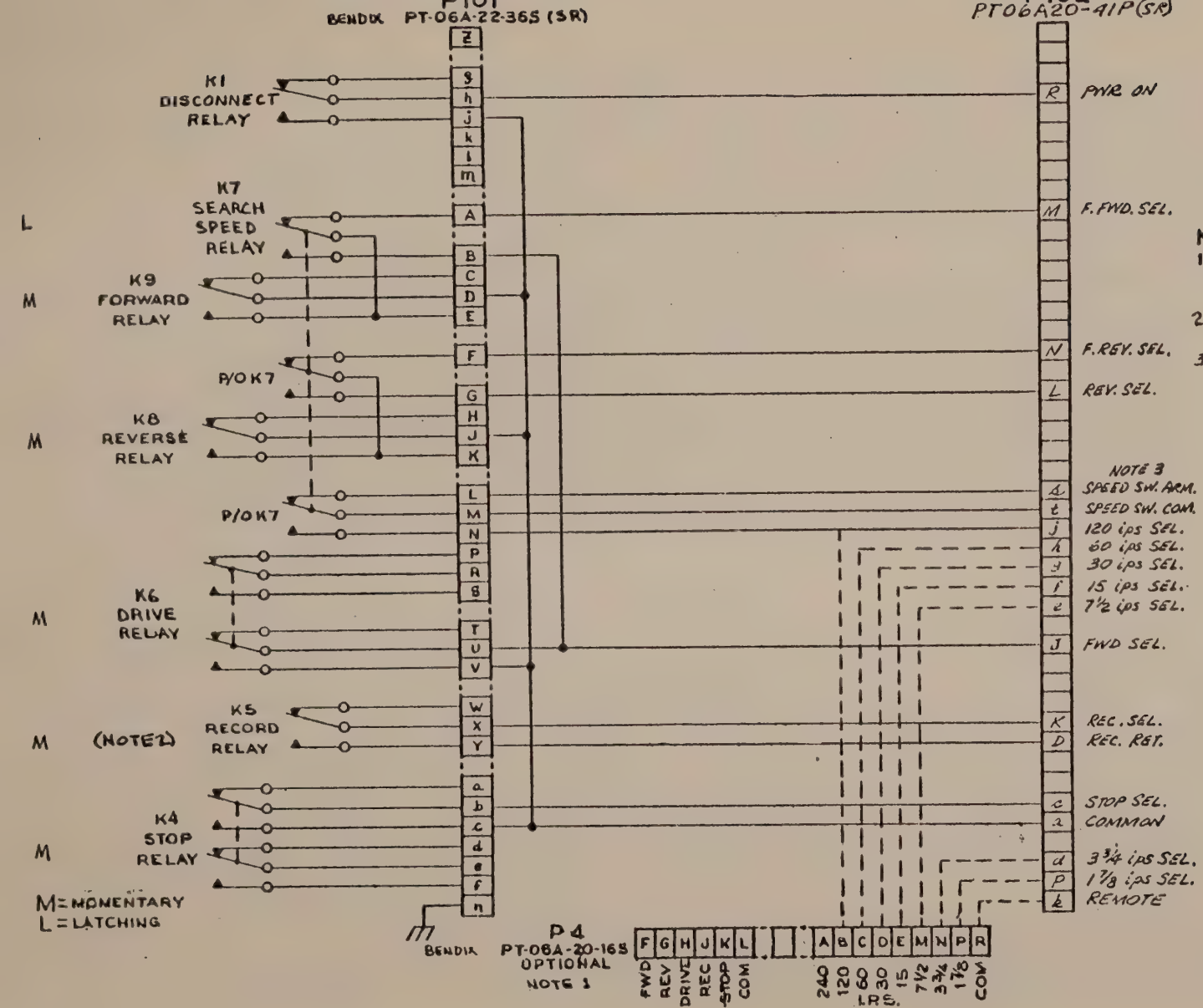
INTERFACE CABLE TO AMPEX PR500 #041335-7-28 REV A



INTERFACE CABLE TO AMPEX SP300 #021942-7-1 REV C



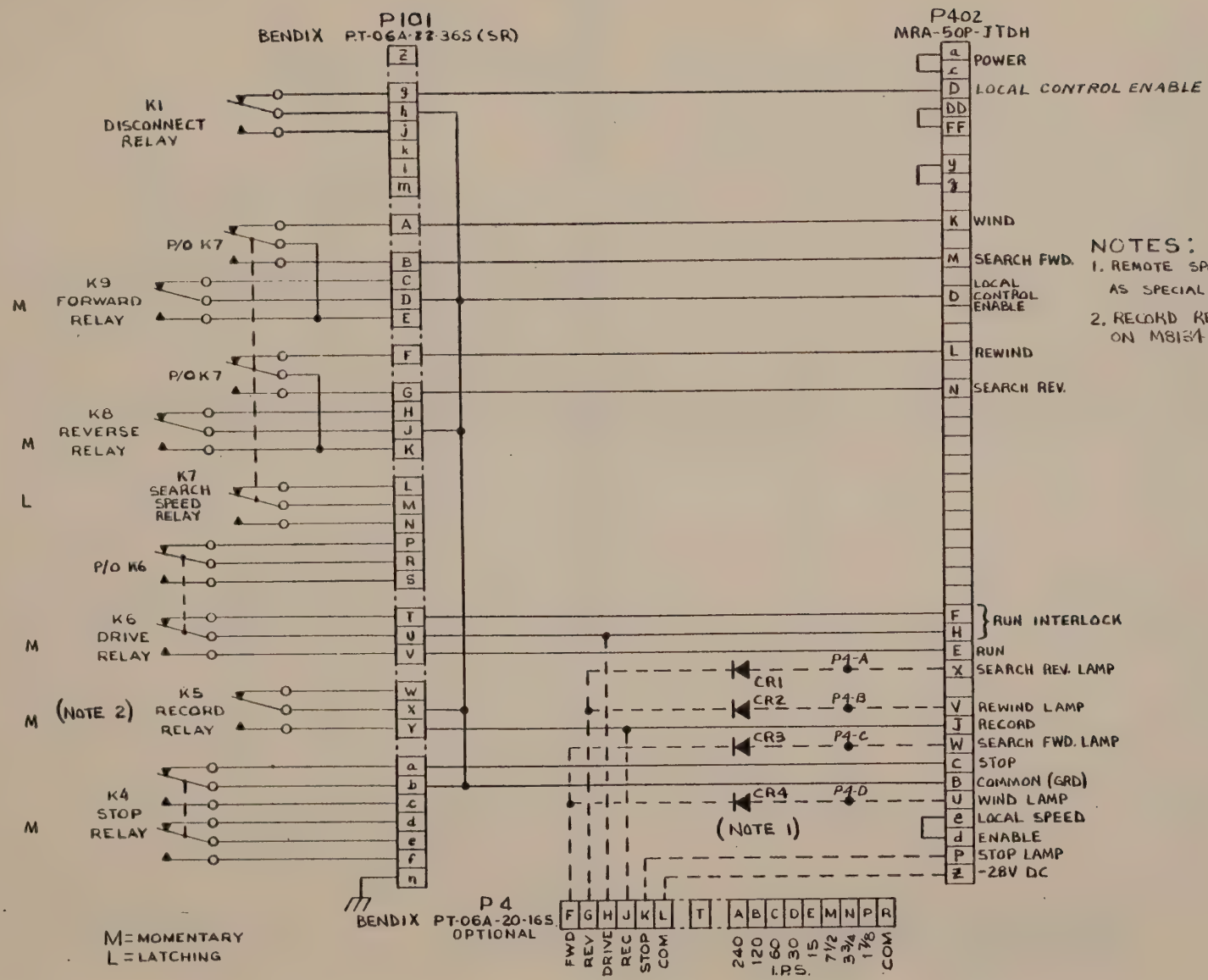
INTERFACE CABLE TO ASTRO-SCIENCE M14C-2 #031644-7-1 REV A



NOTES:

1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134
3. THE M14G TRANSPORT MUST BE MODIFIED TO MAKE IT POSSIBLE TO SEARCH AT 120 ips CONTROLLED SPEED. DISCONNECT THE M14G SPEED SWITCH ARM FROM THE COMMON LINE (ITS NORMAL DESTINATION WITHIN THE M14G). CONNECT THE ARM TO J16-A AND THE COMMON TO J16-t.

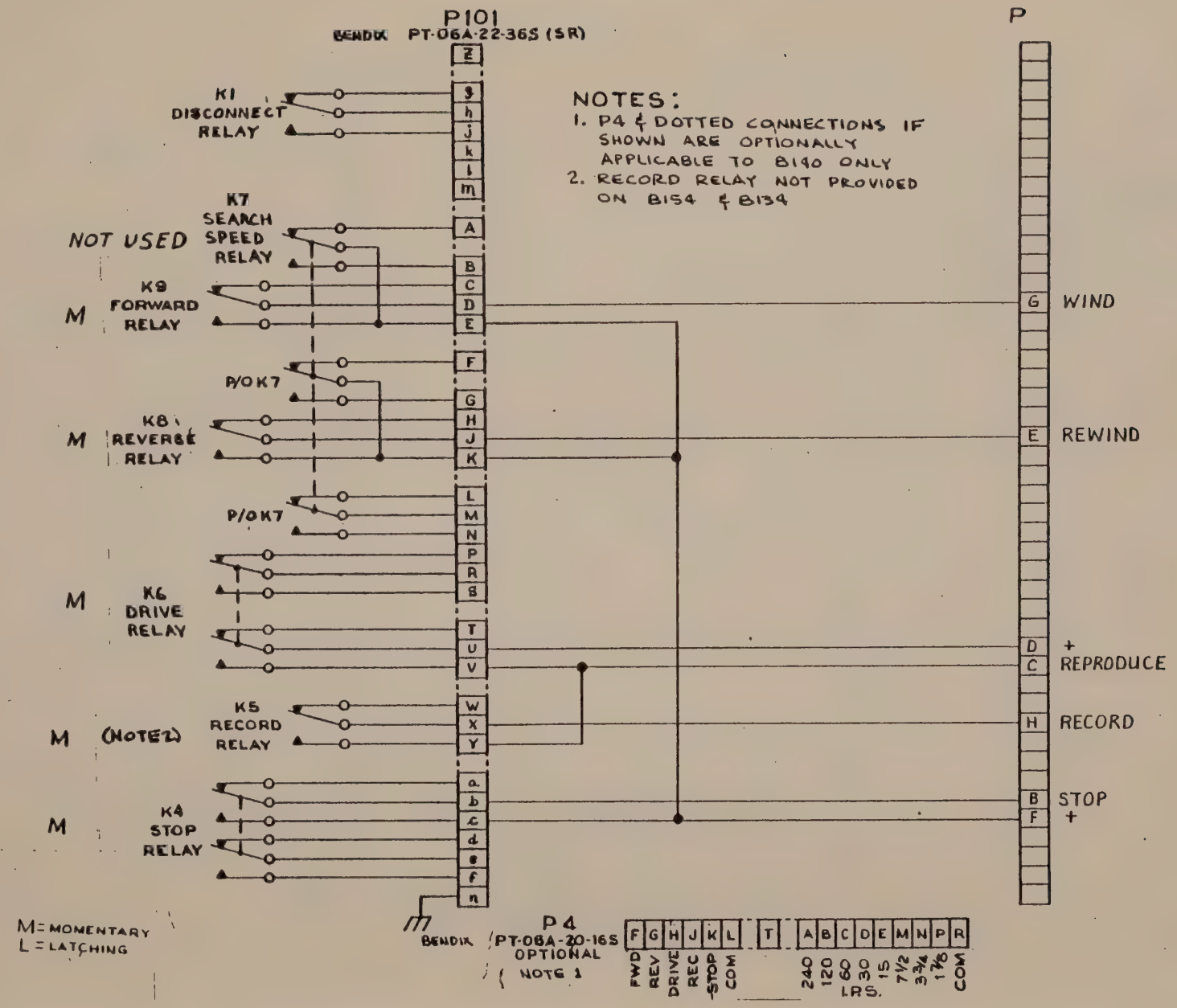
INTERFACE CABLE TO ASTRO-SCIENCE M14G #041335-7-81 REV A_1



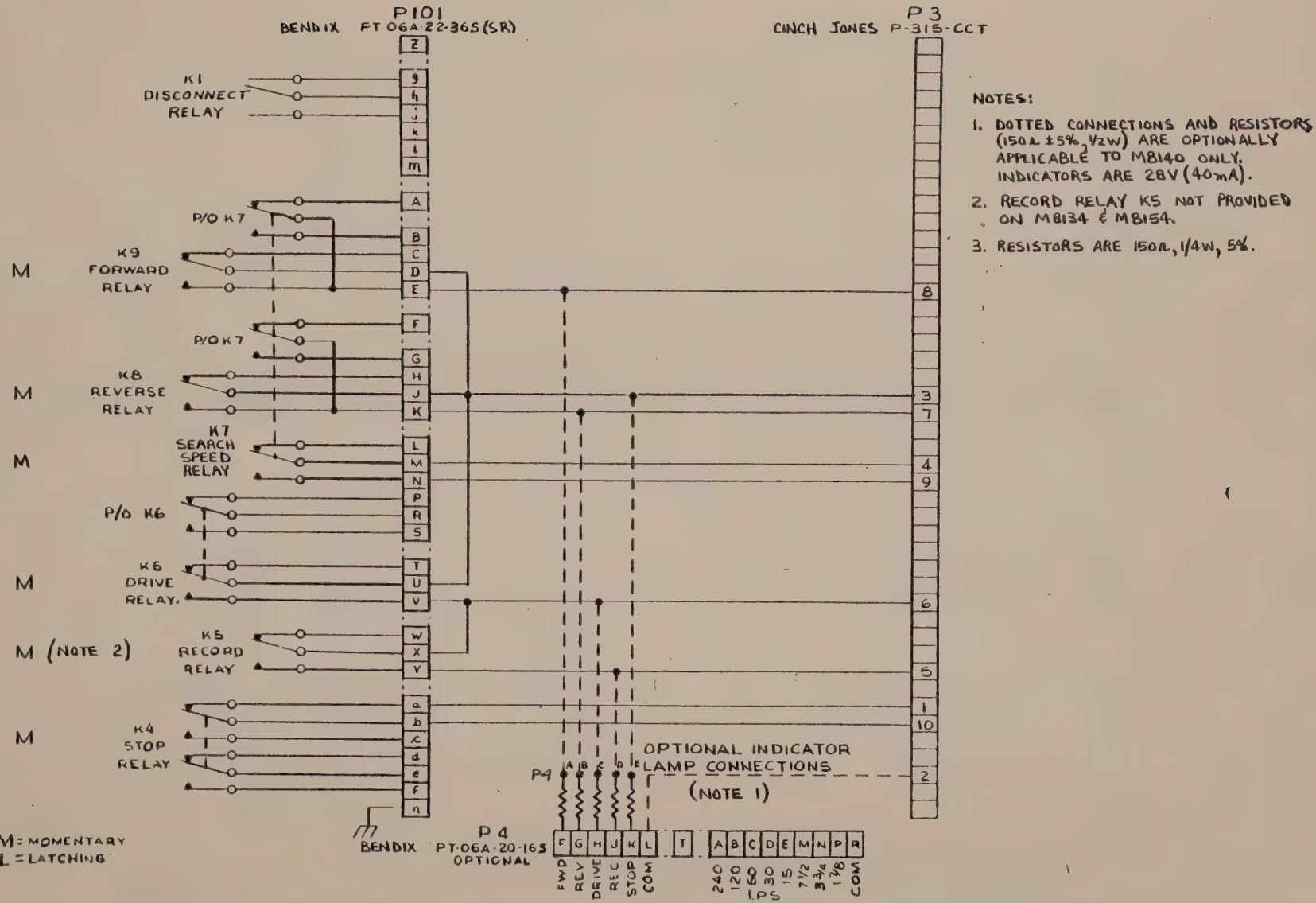
NOTES:

1. REMOTE SPEED SELECTION AVAILABLE AS SPECIAL OPTION ON M8140 ONLY
2. RECORD RELAY K5 NOT PROVIDED ON M8151 & M8154.

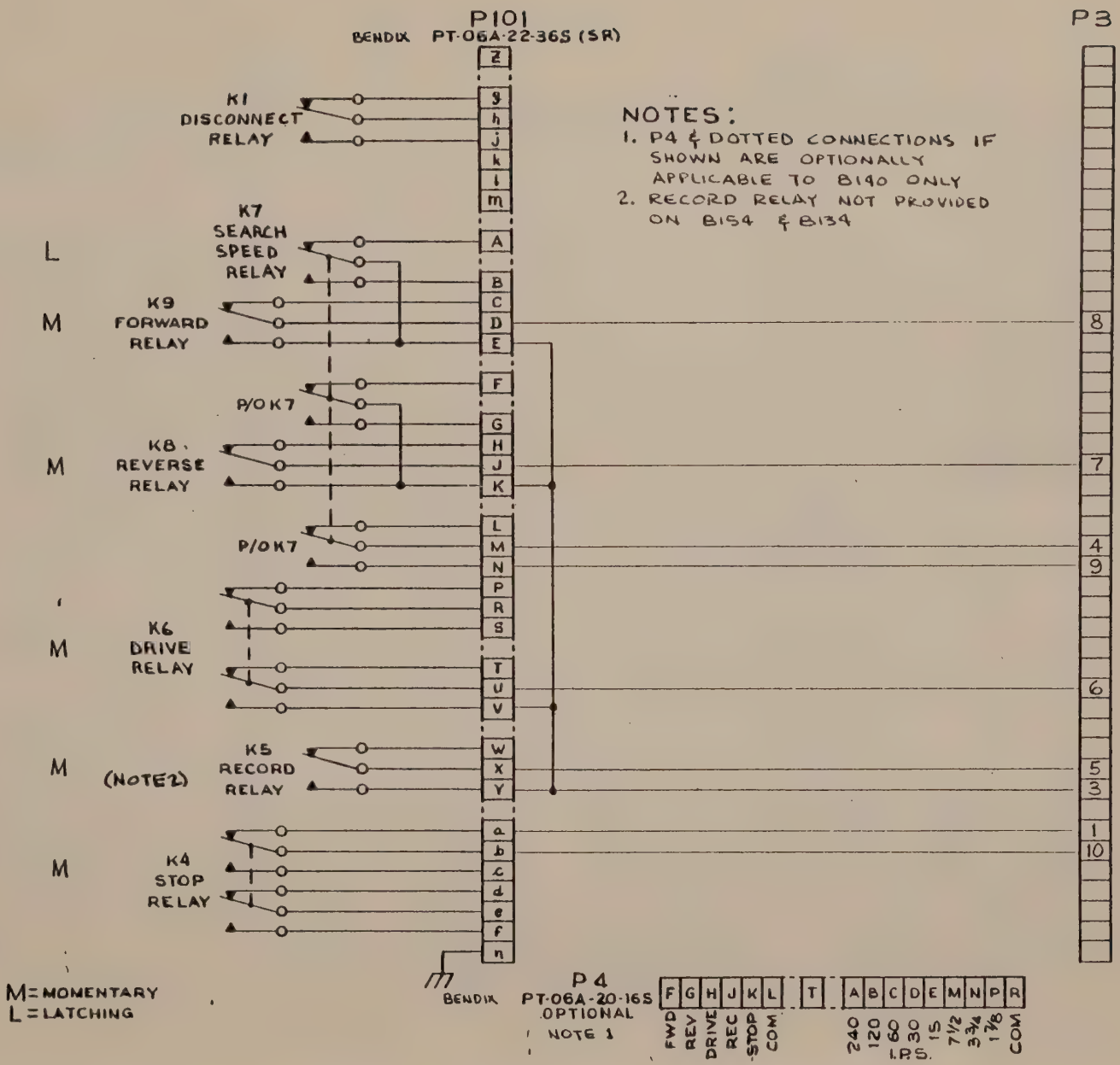
INTERFACE CABLE TO BELL & HOWELL (CEC) VR2600/VR3600 #031048-7-1 REV C



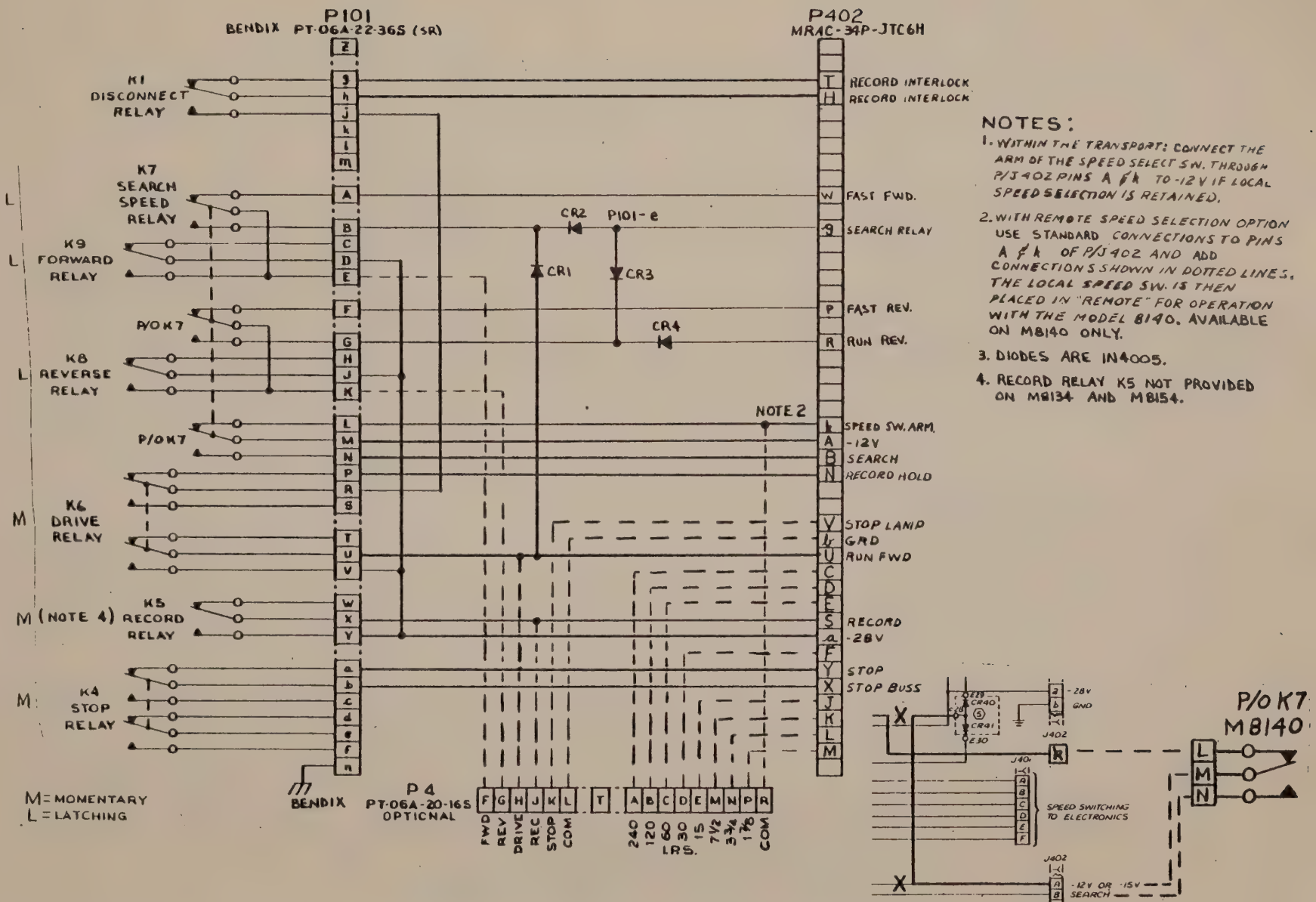
INTERFACE CABLE TO BELL & HOWELL VR3200 #041335-7-58 REV A



INTERFACE CABLE TO BELL & HOWELL (CEC) VR3300 #021946-7 REV C



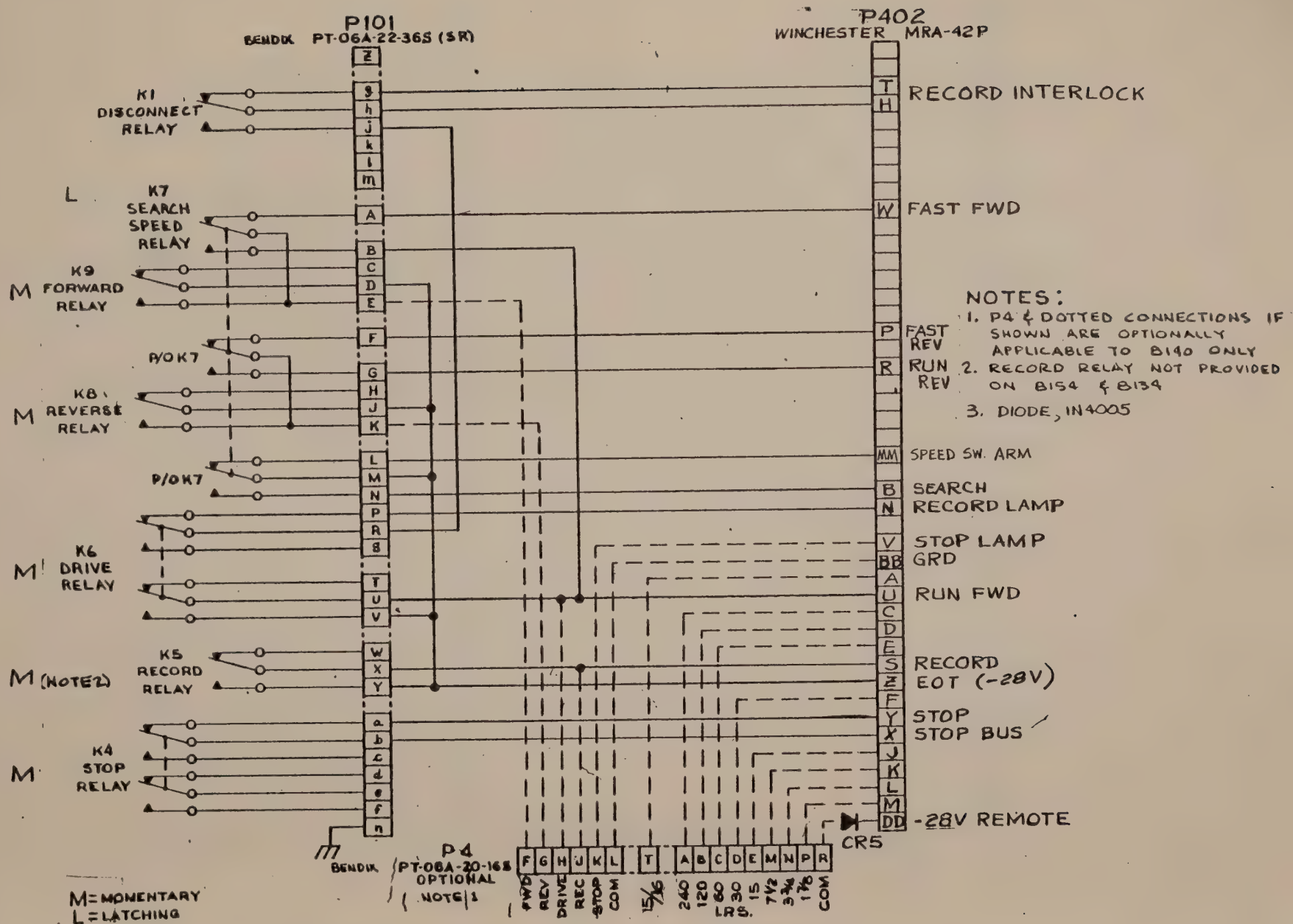
INTERFACE CABLE TO BELL & HOWELL VR3360 #041335-7-64 REV B



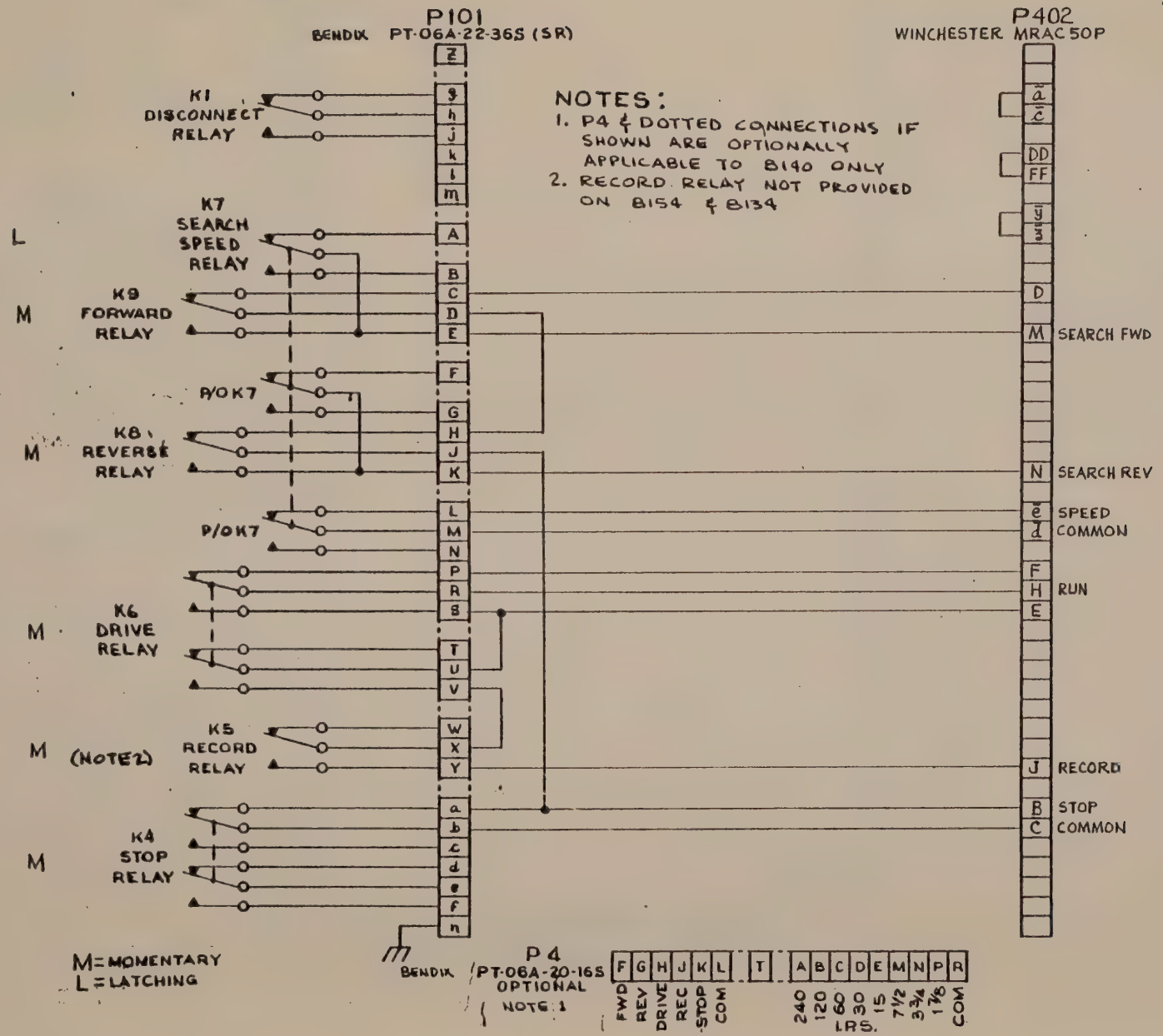
NOTES:

1. WITHIN THE TRANSPORT: CONNECT THE ARM OF THE SPEED SELECT SW. THROUGH P/J402 PINS A & k TO -12V IF LOCAL SPEED SELECTION IS RETAINED.
2. WITH REMOTE SPEED SELECTION OPTION USE STANDARD CONNECTIONS TO PINS A & k OF P/J402 AND ADD CONNECTIONS SHOWN IN DOTTED LINES. THE LOCAL SPEED SW. IS THEN PLACED IN "REMOTE" FOR OPERATION WITH THE MODEL 8140. AVAILABLE ON M8140 ONLY.
3. DIODES ARE IN4005.
4. RECORD RELAY K5 NOT PROVIDED ON M8134 AND M8154.

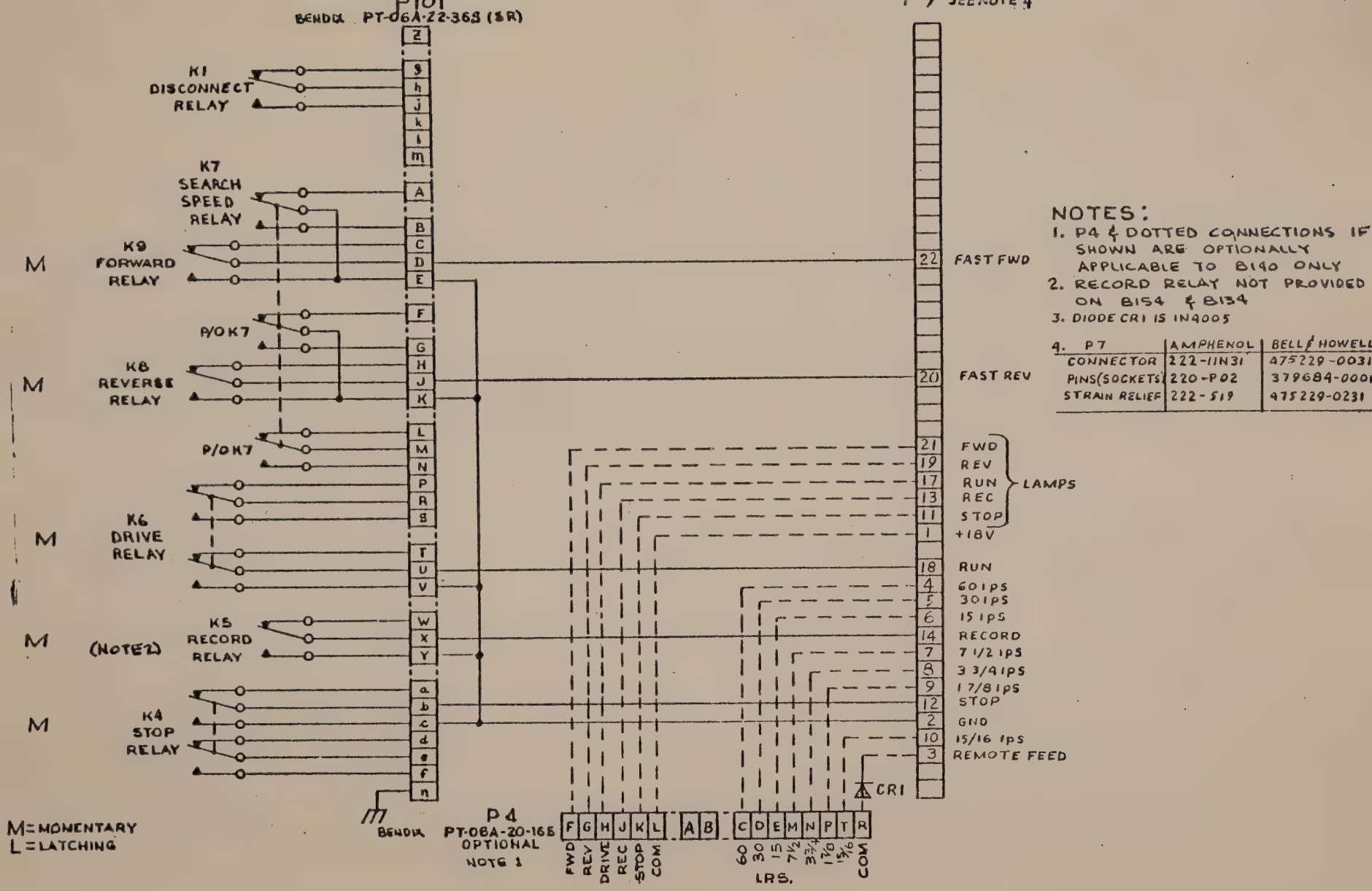
INTERFACE CABLE TO BELL & HOWELL (CEC) VR3400/VR3700A #031323-7-1 REV D



INTERFACE CABLE TO BELL & HOWELL (CEC) VR3700B #041335-7-37 REV B



INTERFACE CABLE TO BELL & HOWELL (CEC) VR3800 #041335-7-66 REV A

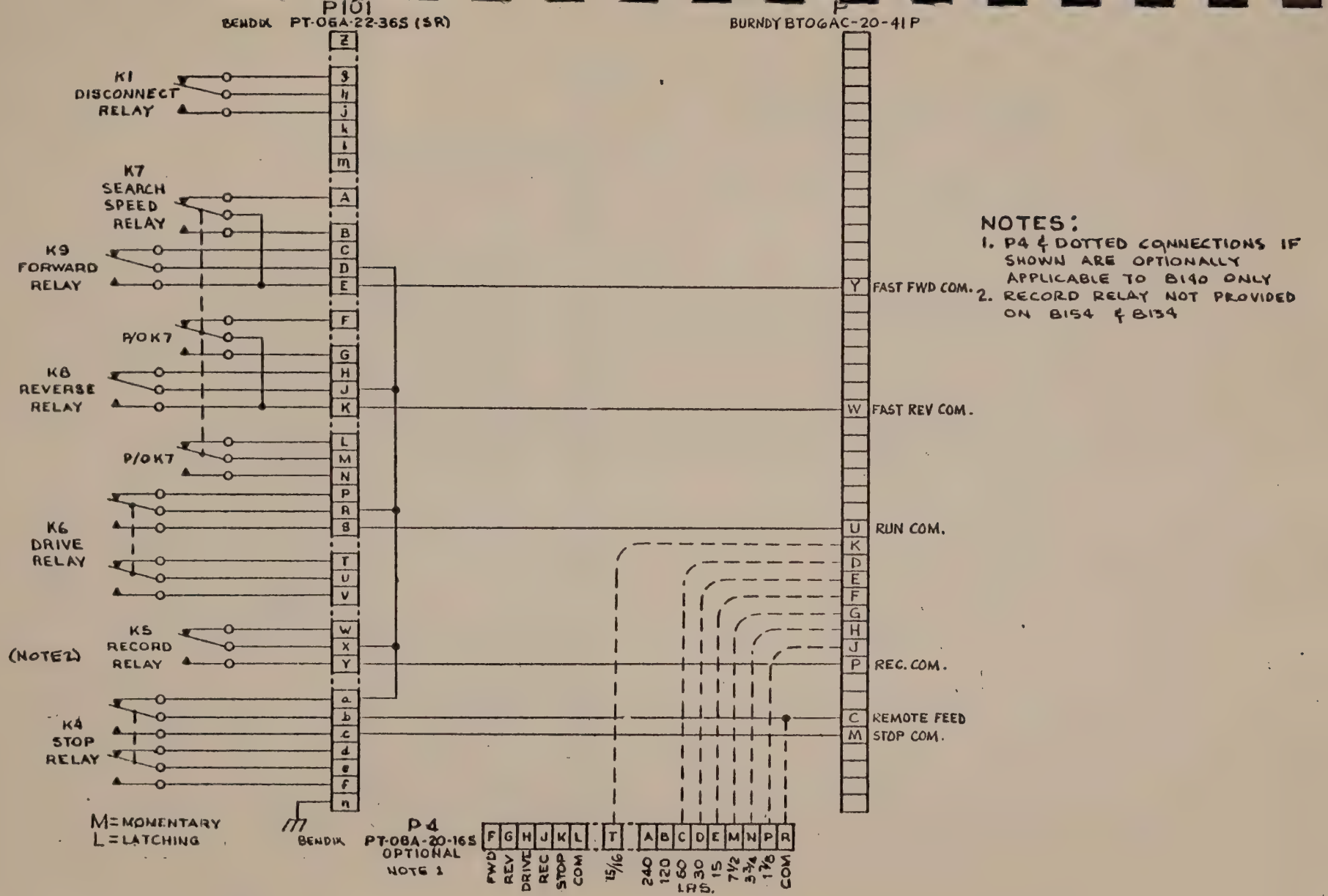


NOTES:

1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134
3. DIODE CR1 IS IN4005
4. P7

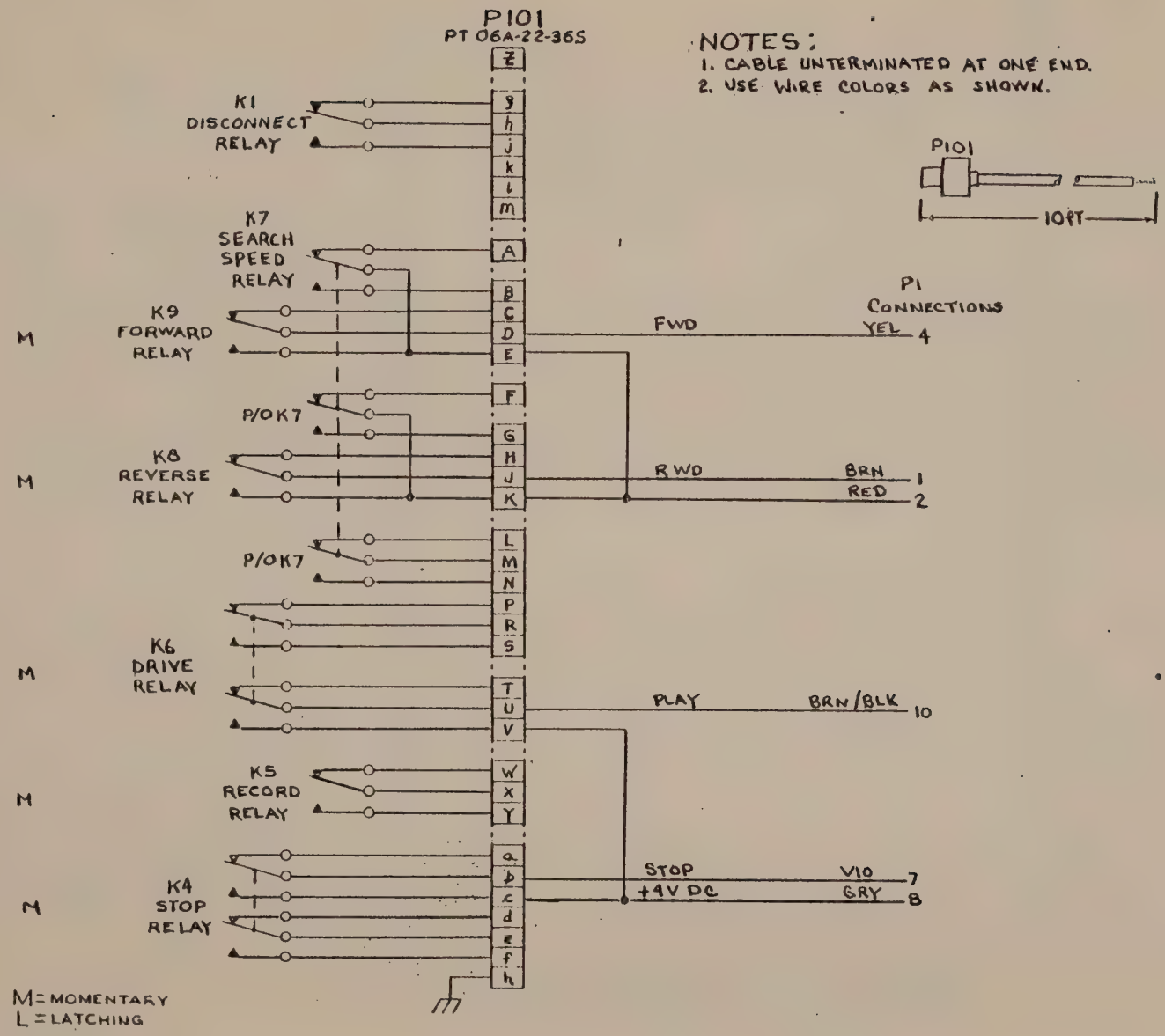
	AMPHENOL	BELL & HOWELL
CONNECTOR	222-11N31	475229-0031
PINS(SOCKETS)	220-P02	379684-0001
STRAIN RELIEF	222-519	475229-0231

INTERFACE CABLE TO BELL & HOWELL CPR4010 #041335-7-50 REV A

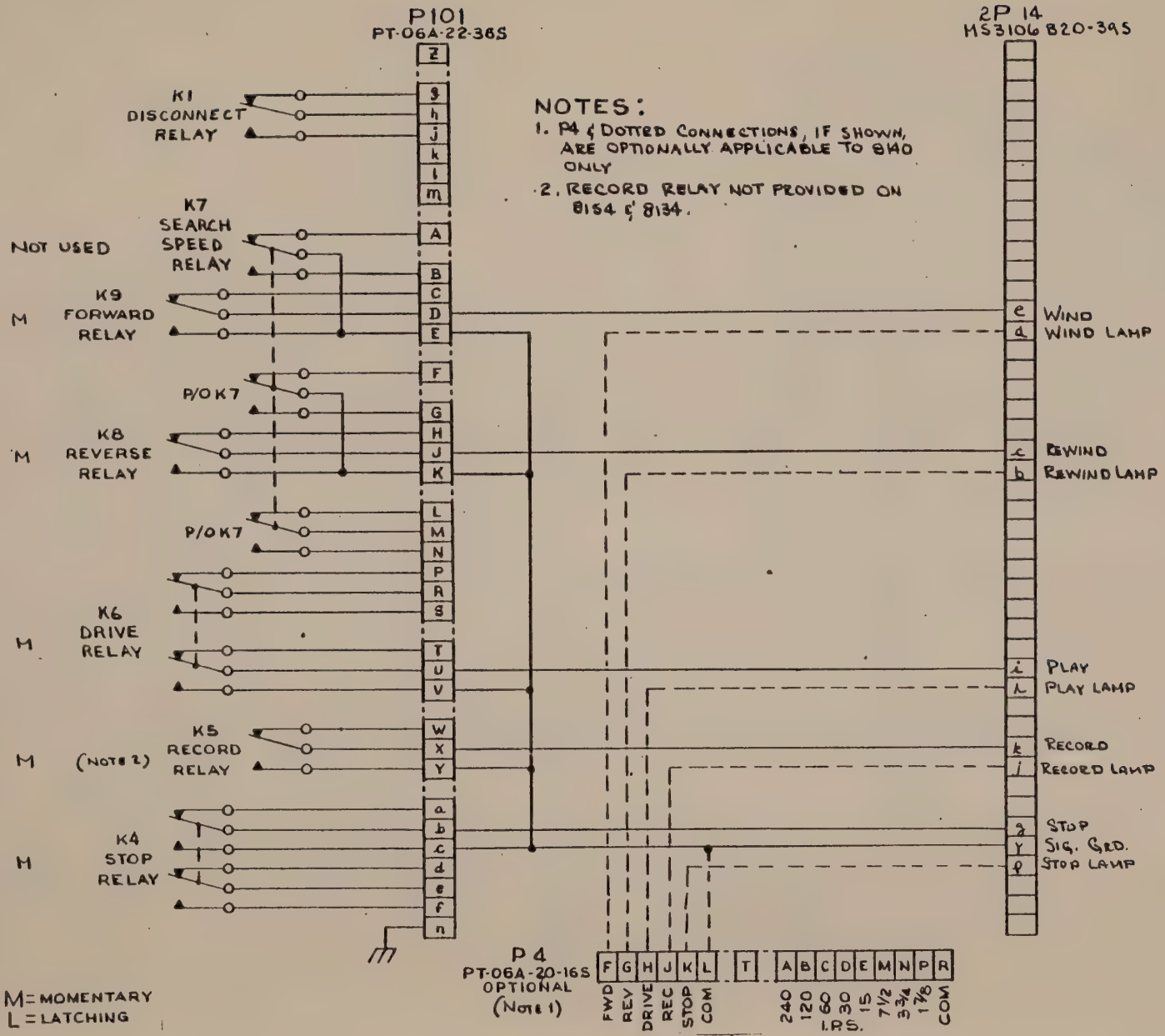


NOTES:
1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134

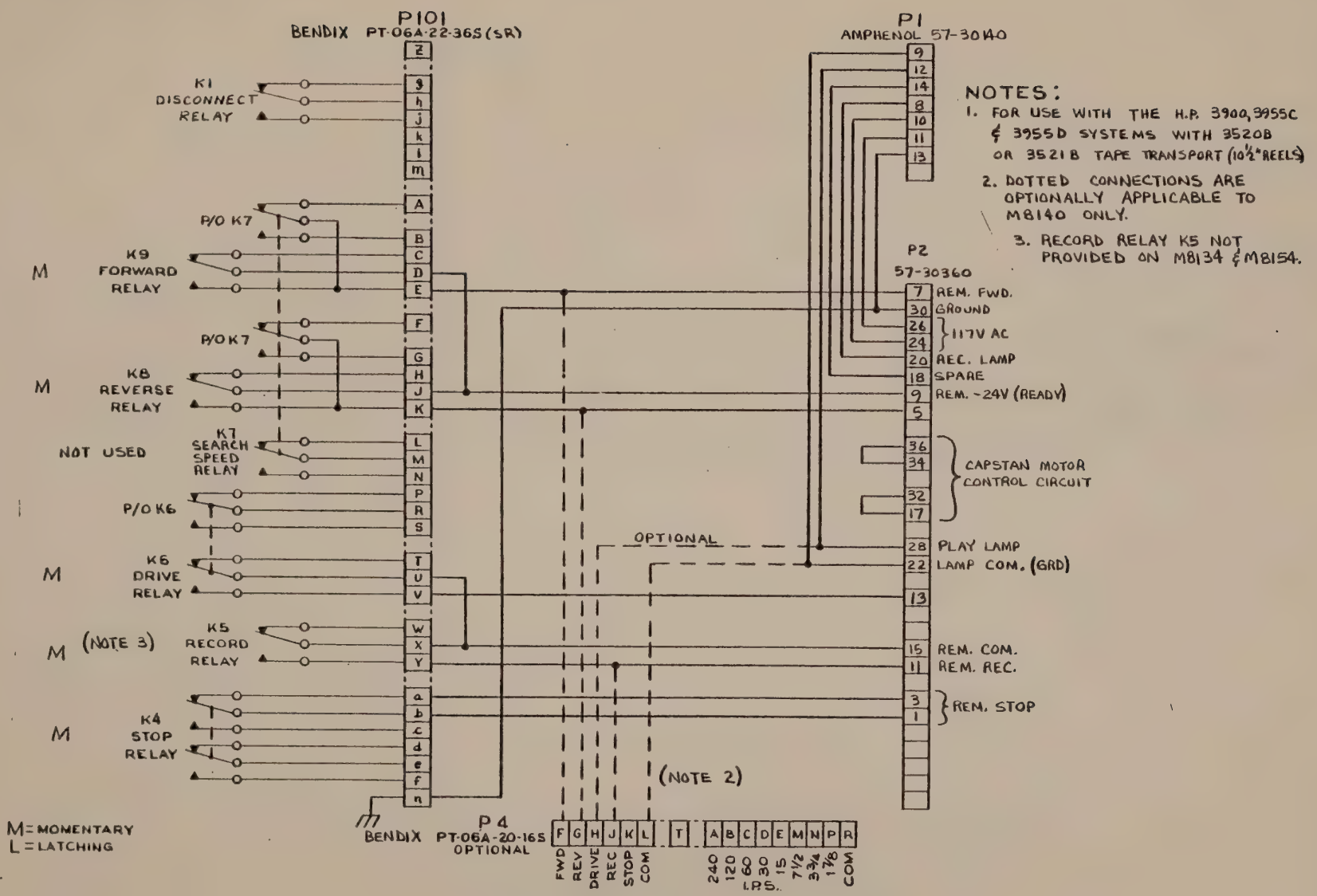
INTERFACE CABLE TO BELL & HOWELL 12-401B #041335-7-74 REV A_1



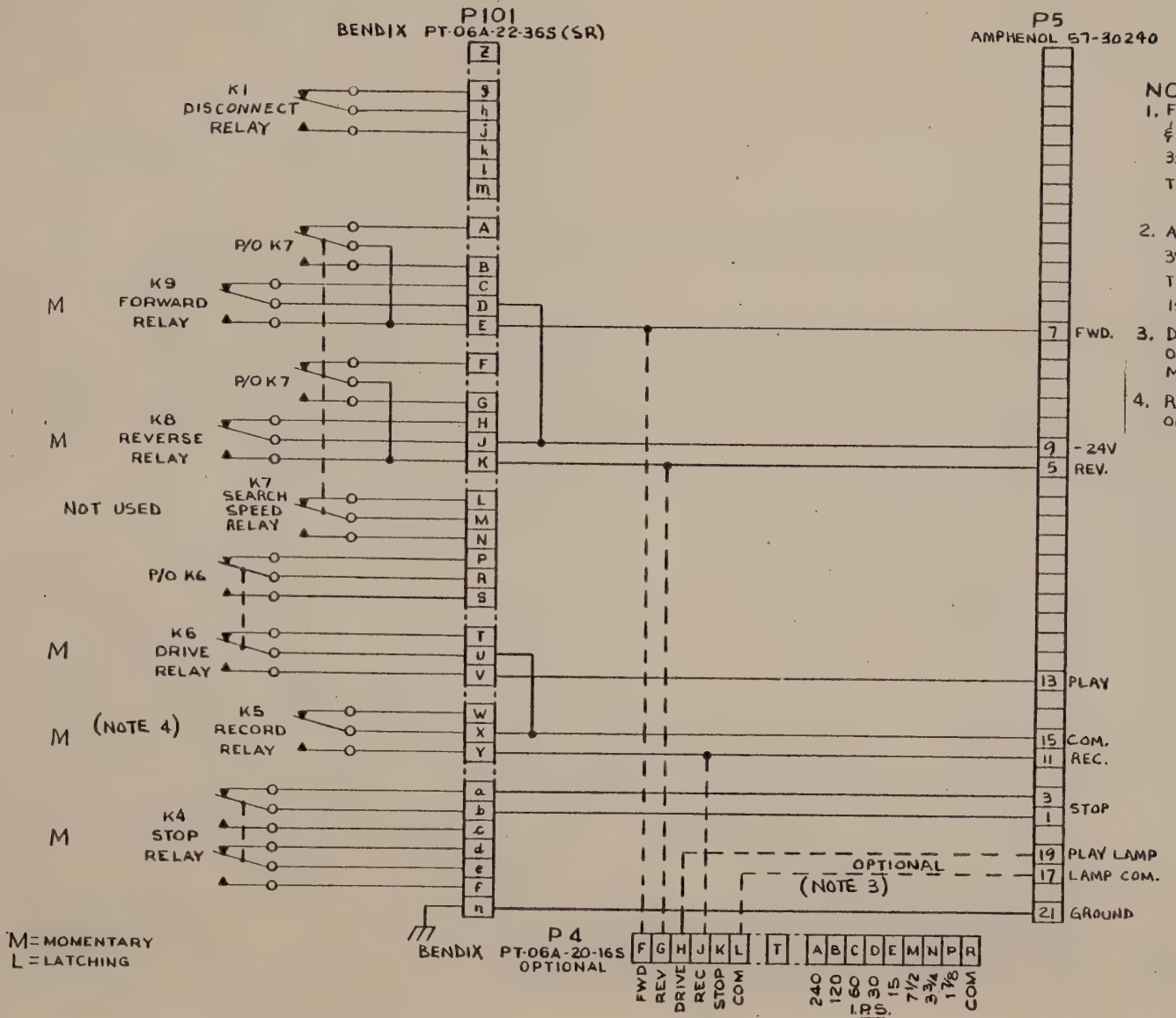
INTERFACE CABLE TO CROWN RC40 #041335-7-36



INTERFACE CABLE TO GENISCO 10-276 #041335-7-29



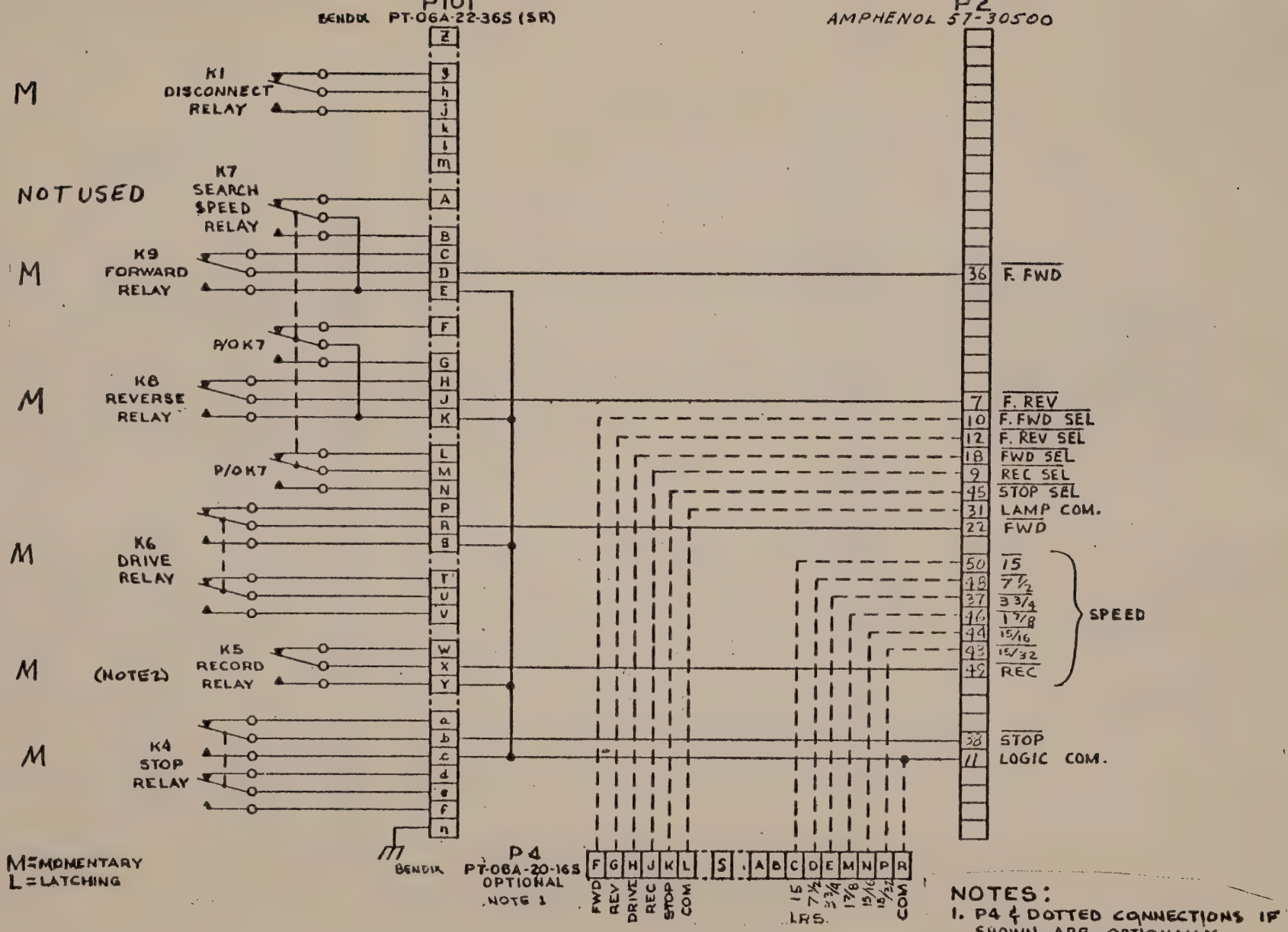
INTERFACE CABLE TO HEWLETT-PACHARD 3900/3955C/3955D #021978 REV C



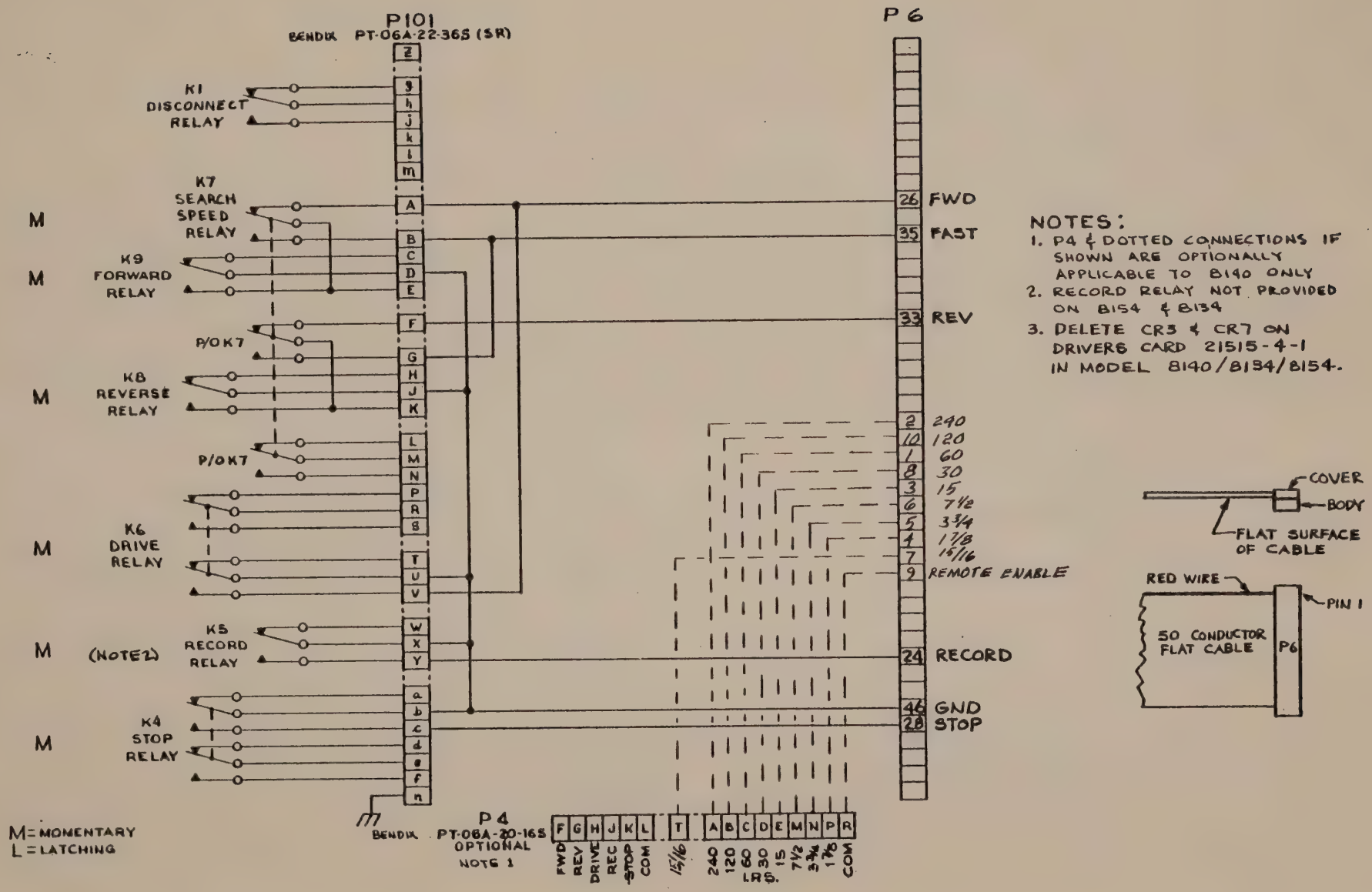
NOTES:

1. FOR USE WITH THE H.P. 3950, 3955A & 3955B SYSTEMS WITH 3524A, 3525A, 3526A OR 3527A TAPE TRANSPORT (15" REELS)
2. ALSO USED WITH THE H.P. 3900, 3955C & 3955D SYSTEMS WHEN THE MODEL 3681A TAPE SERVO IS USED.
3. DOTTED CONNECTIONS ARE OPTIONALLY APPLICABLE TO M8140 ONLY.
4. RECORD RELAY K5 NOT PROVIDED ON M8134 & M8154.

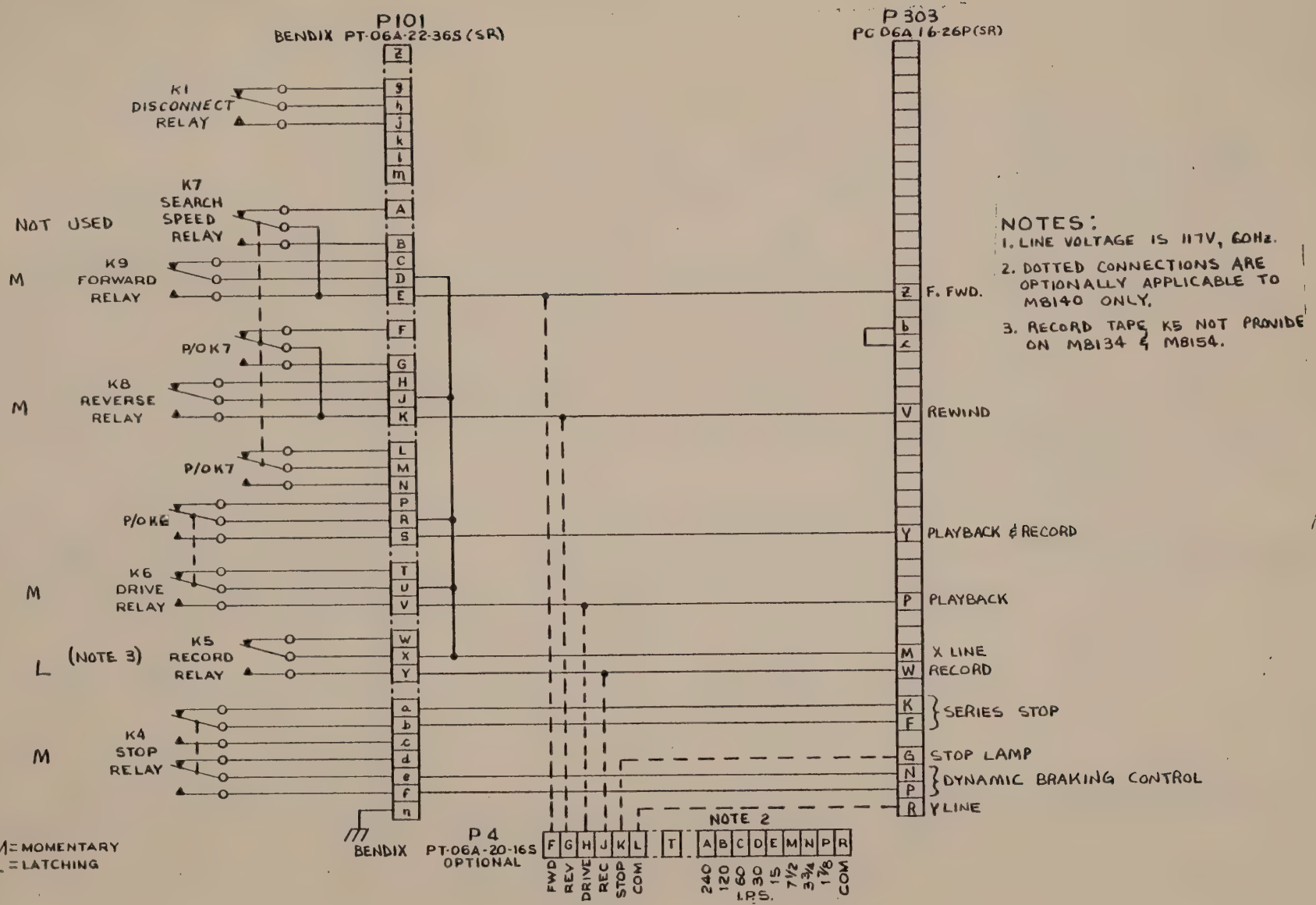
INTERFACE CABLE TO HEWLETT-PACHARD 3950/3955A/3955B #021977-7-1 REV C



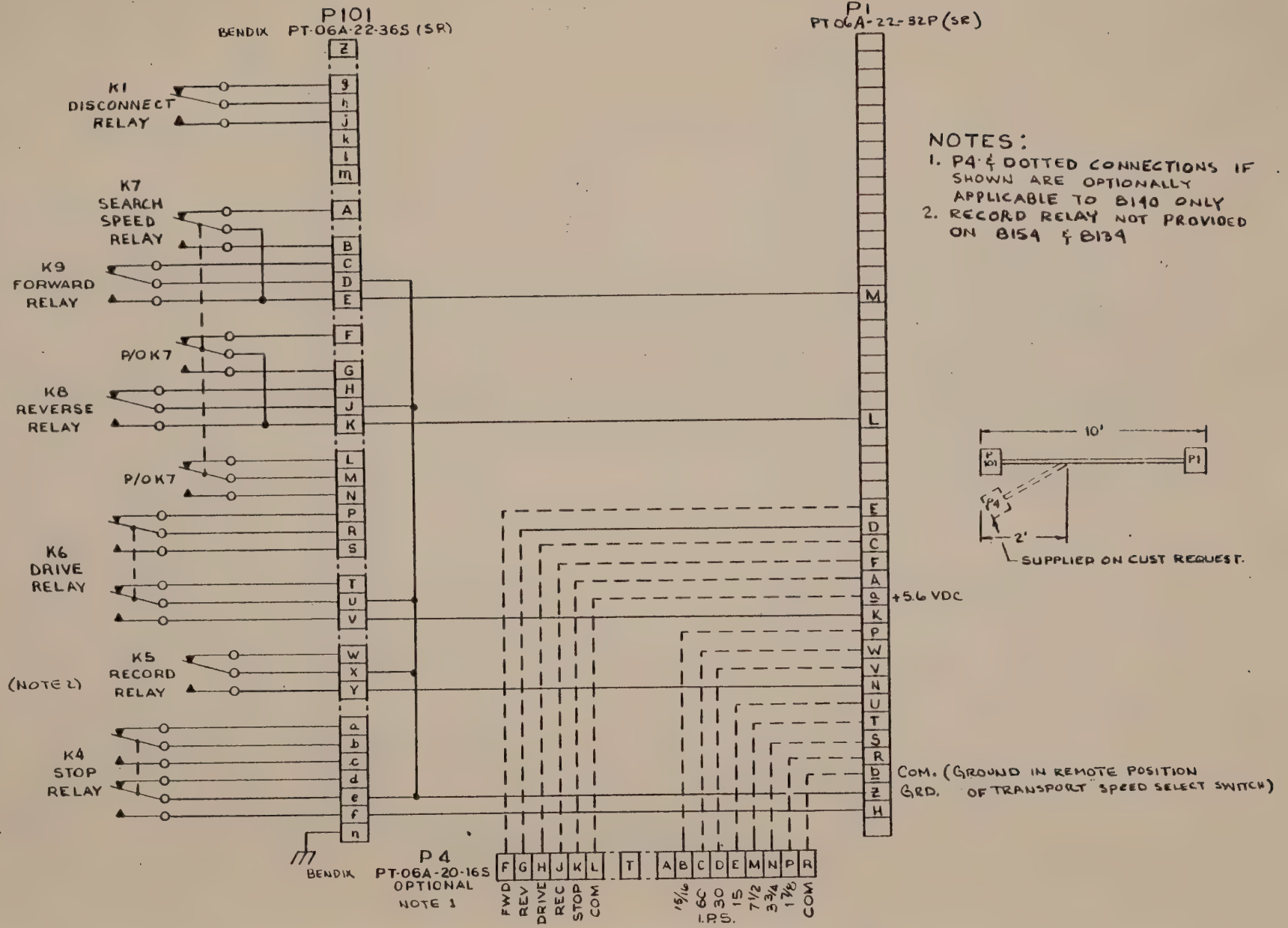
INTERFACE CABLE TO HEWLETT-PACHARD 3964A/3968A #041335-7-97



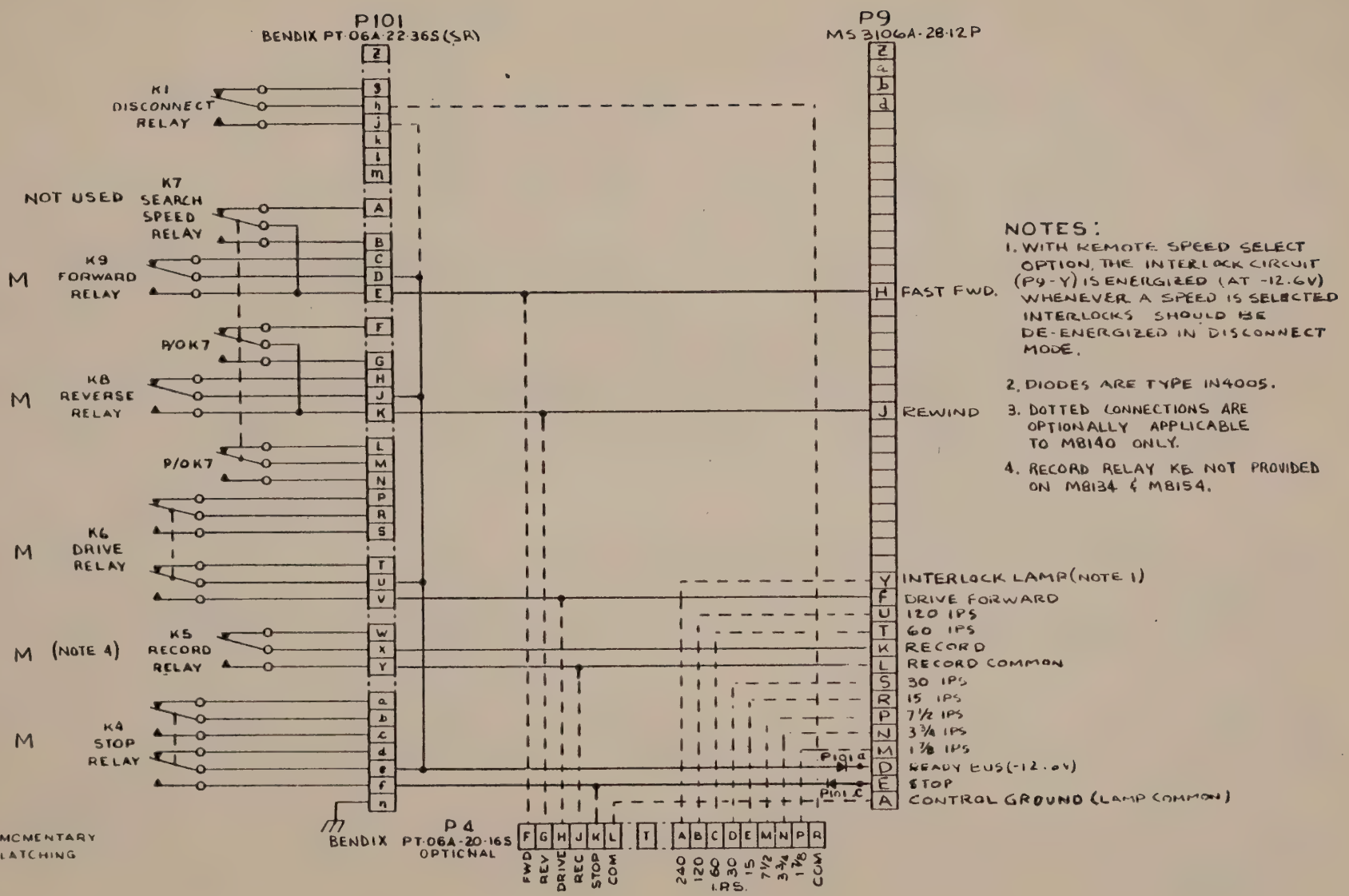
INTERFACE CABLE TO HONEYWELL 96 #041335-7-47 REV B



INTERFACE CABLE TO HONEYWELL 3175 #031087-7-1 REV B



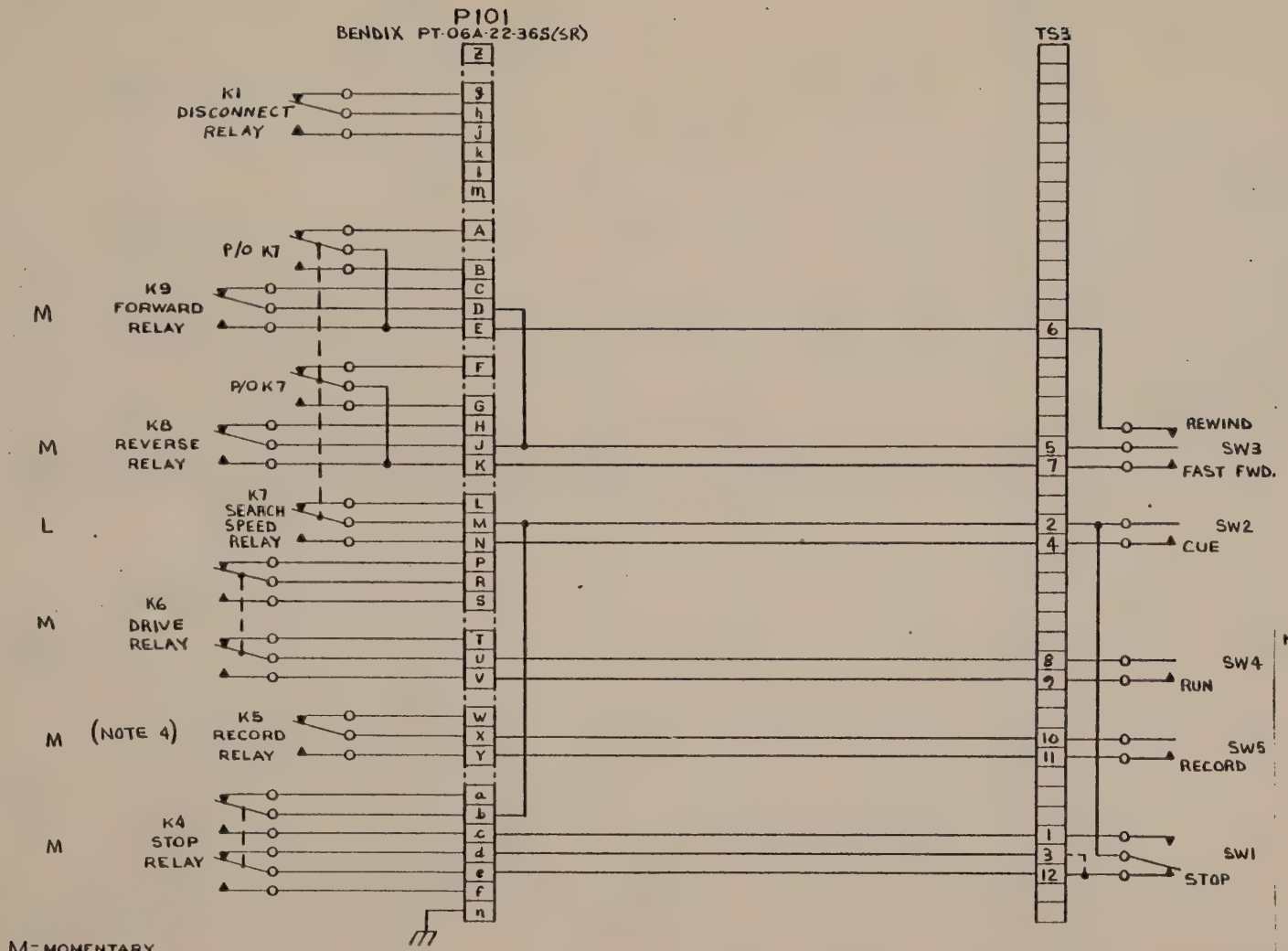
INTERFACE CABLE TO HONEYWELL 5600 #041335-7-32 REV A



NOTES:

1. WITH REMOTE SPEED SELECT OPTION, THE INTERLOCK CIRCUIT (P9-Y) IS ENERGIZED (AT -12.6V) WHENEVER A SPEED IS SELECTED INTERLOCKS SHOULD BE DE-ENERGIZED IN DISCONNECT MODE.
2. DIODES ARE TYPE IN4005.
3. DOTTED CONNECTIONS ARE OPTIONALLY APPLICABLE TO M8140 ONLY.
4. RECORD RELAY K5 NOT PROVIDED ON M8134 & M8154.

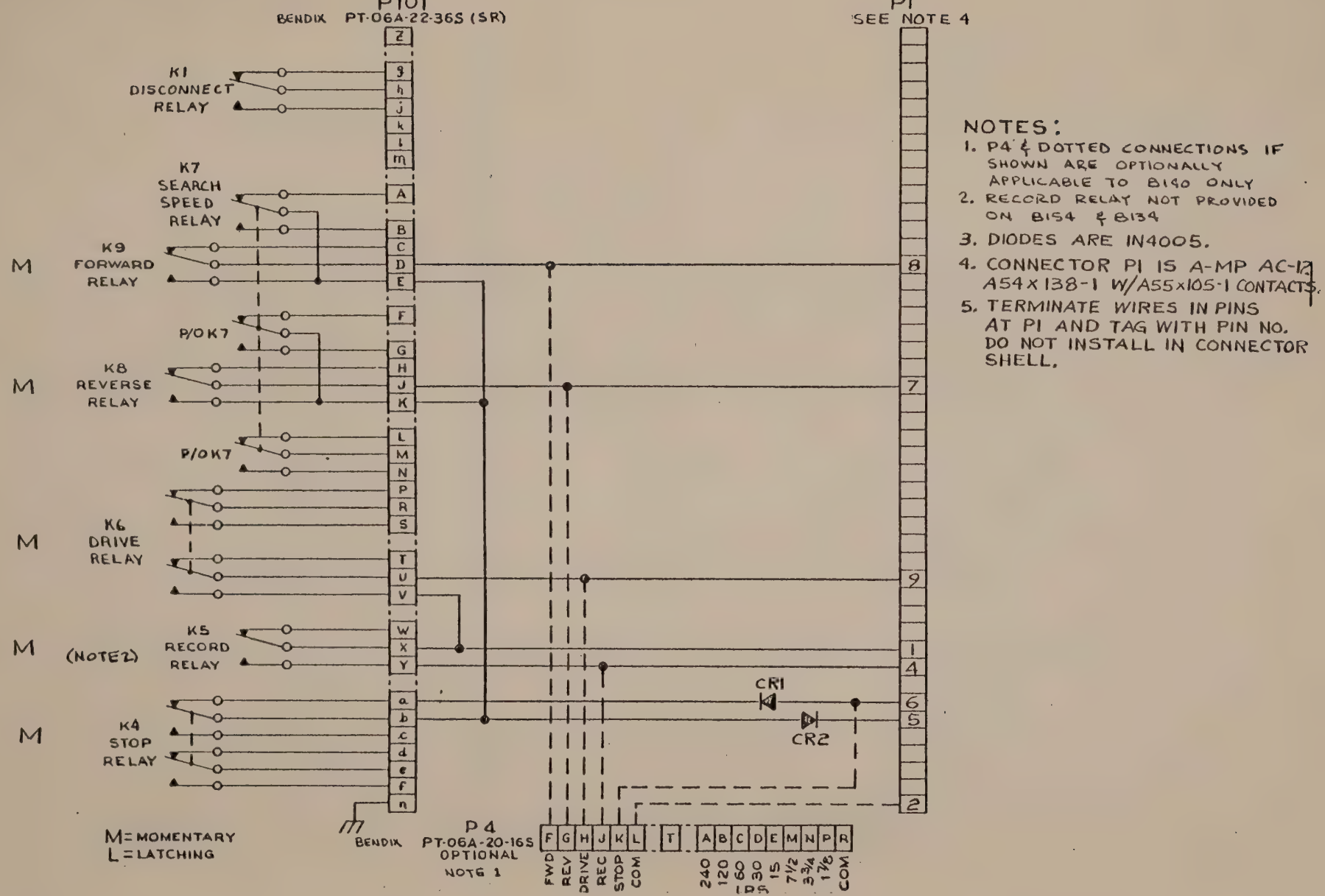
INTERFACE CABLE TO HONEYWELL 7600 #021947-7-1 REV C



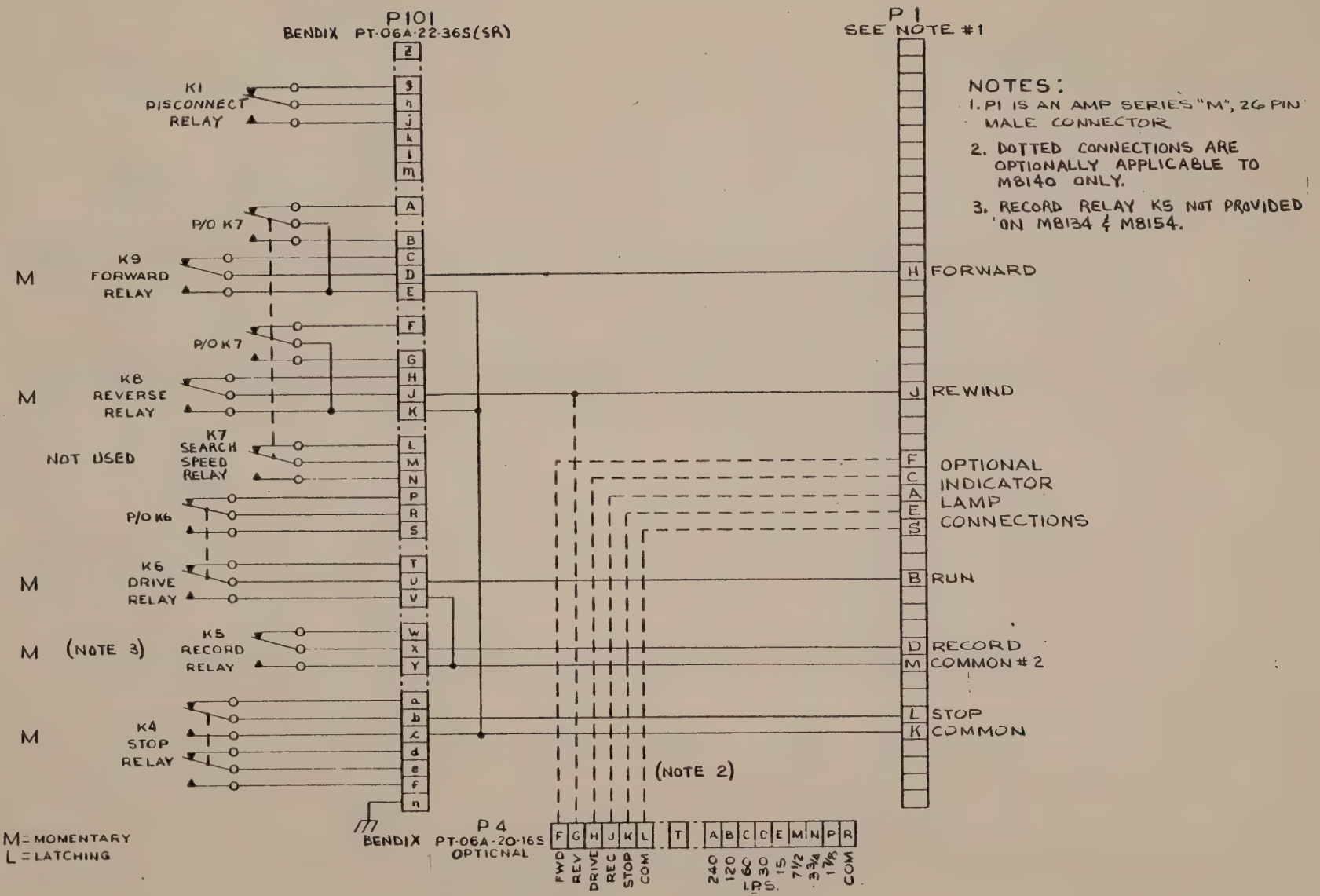
NOTES:

1. REMOVE N.C. CONTACT OF SW1 (STOP) FROM TERM. 3 OF TS3 & CONNECT TO SPARE TERM. 12 AS SHOWN.
2. IF INTERFACE CABLE IS REMOVED, JUMPER TERM. 12 TO TERM. 3 ON TS3 AS SHOWN WITH DOTTED LINE.
3. TERMINATE WIRES TO TS3 WITH LUGS.
4. RECORD RELAY K5 NOT PROVIDED ON M8134 & M8154

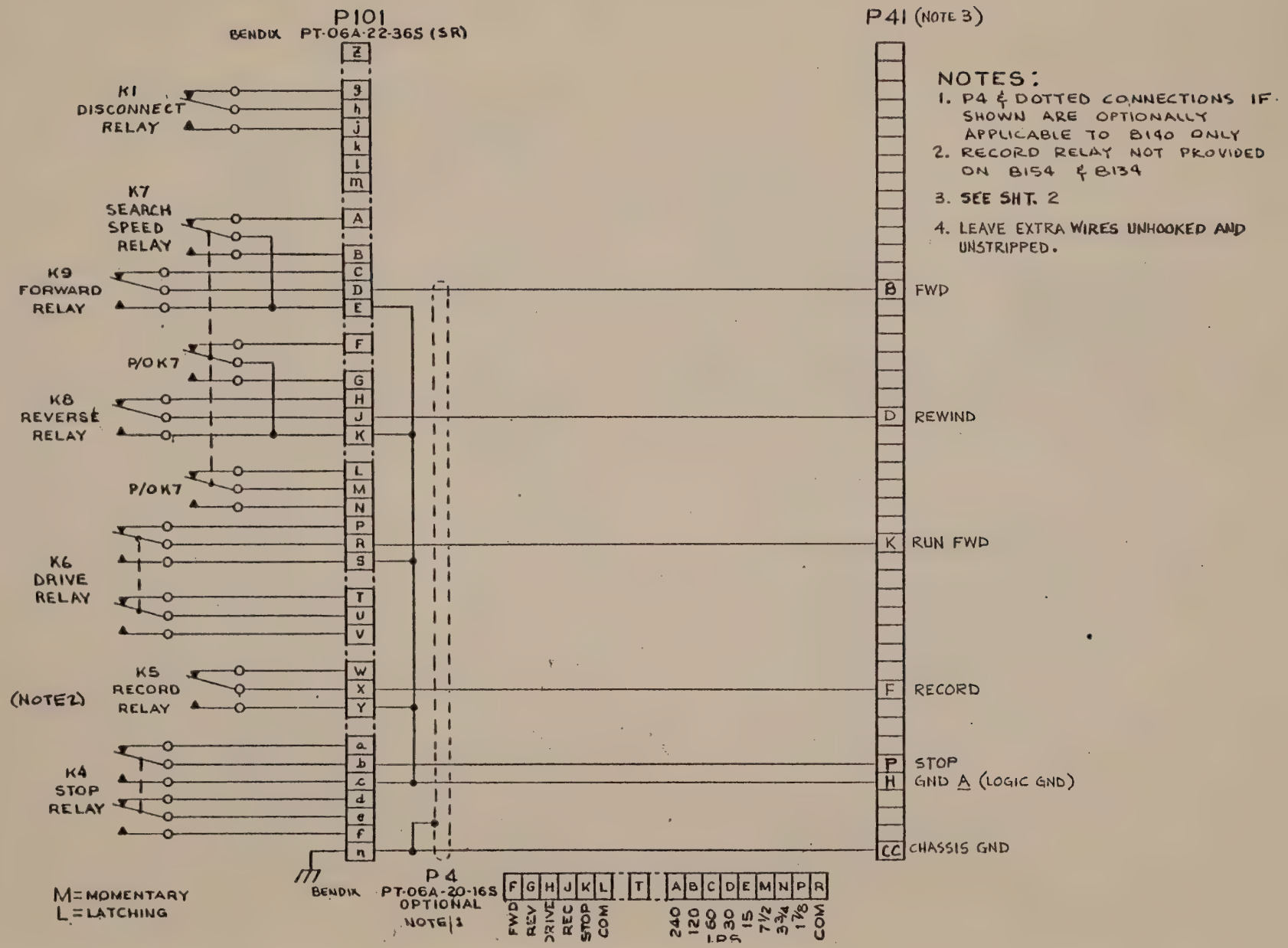
INTERFACE CABLE TO MAGNASYNC TR-1510 #031275-7-1 REV B



INTERFACE CABLE TO MIDWESTERN A434 #041335-7-38 REV A



INTERFACE CABLE TO MINCOM 34 #021948-7 REV C

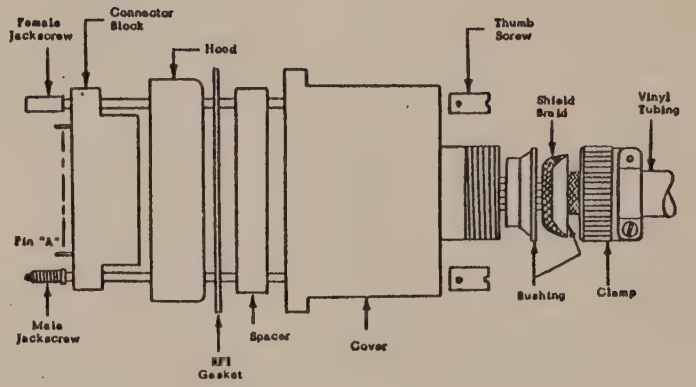


INTERFACE CABLE TO MINCOM 110 #041335-7-42 (Sheet 1 of 2)

PARTS LIST

This list contains parts for a fully shielded (RFI) connector to mate with the remote control connector mounted on the Series 110.

ITEM	QTY.	DESCRIPTION	3M CATALOG NO.
1	1	Connector shell, AMP Inc., number 201358-3 (50 positions)	83-1610-0673
2	1	Adapter, RF cable, M50/M34 connector, Sunbank Elect. Inc., No. J766-50	83-1610-1577
3	1	Hood, connector, AMP Inc., number 201390-2	83-1610-1576
4	5	Pin, contact, AMP Inc., No. 42992-1 (16-18 gauge wire)	83-1610-0677
5	45	Pin, contact, AMP Inc., No. 42980-1-LP (20-24 gauge wire)	83-1610-0688
6	A/R	22 gauge wire, MIL-W-16878 or equivalent	83-7910-0043
7	A/R	Tubing, blk. vinyl, 0.625ID, 3M No. 3025-080-Blk. or equivalent	83-7910-0291
8	A/R	Shield, braid, 0.625ID, alpha wire No. 2148 or equivalent	83-7910-0404
9	A/R	Wire, twisted, shielded pair, 22 gauge national wire No. NB1934N25J or equivalent	83-7910-0362
10	A/R	Wire, twisted, shielded pair, 16 gauge national wire No. NB192N25J or equivalent	83-7910-0253
11		Assembly tools	
	1	Pin Extractor Tool, AMP No. 305183	NONE
	1	Crimp tool, AMP No. 90012	NONE
12		Hardware	
	4	4-40 X 3/8 cap screw	NONE
	4	#4 flat washer, small pattern	NONE
	4	#4 split washer, small pattern	NONE
	4	#4 Hex nut, small pattern	NONE
13		If a non-RFI cable is wanted, items 2 and 8 can be deleted, but the following items should be added;	
	1	Jackscrew, male, AMP No. 200868-2	83-9262-0353
	1	Jackscrew, female, AMP No. 200870-2	83-9262-0354
	1	Shell, AMP No. 201443 or 201386	NONE

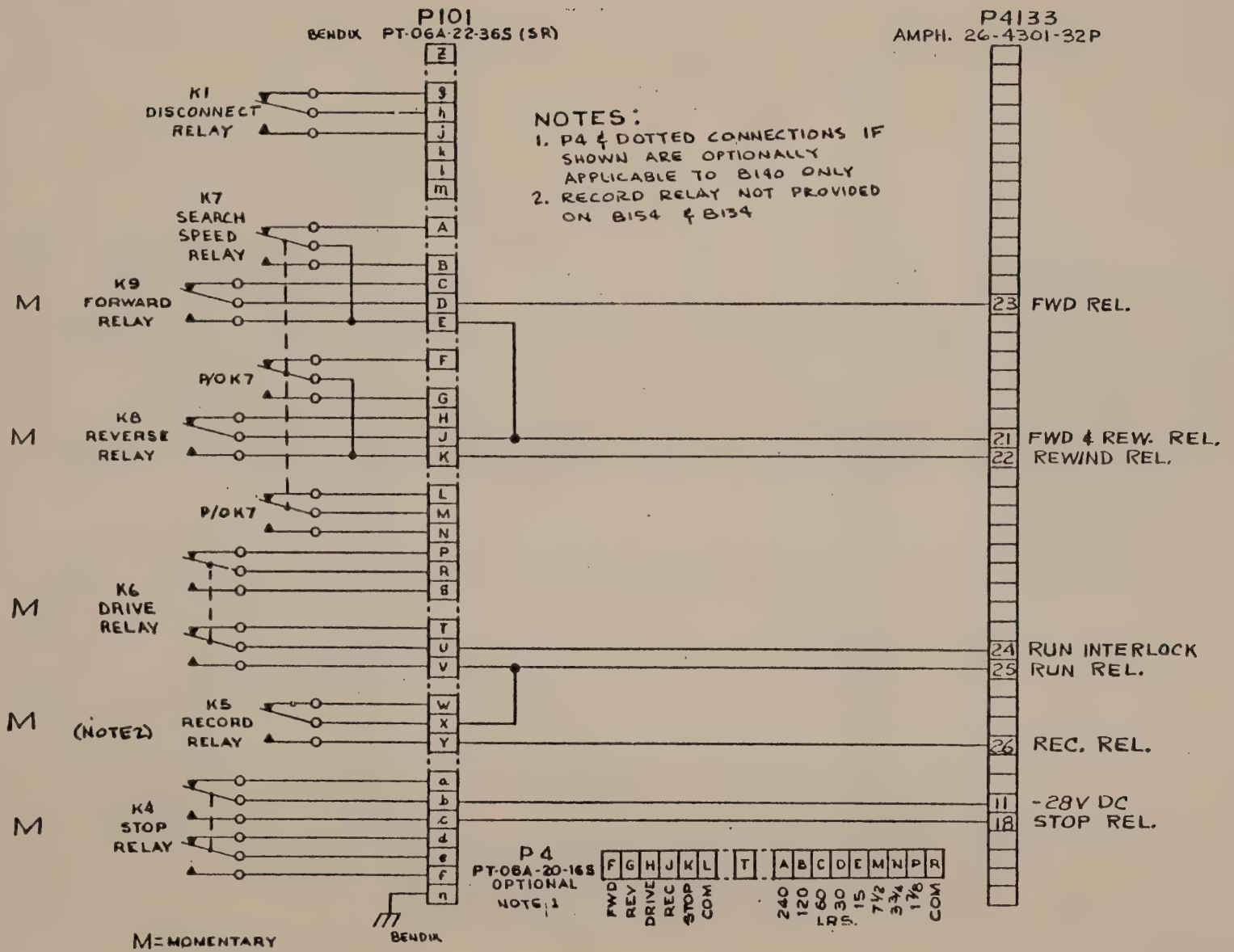


ASSEMBLY PROCEDURE

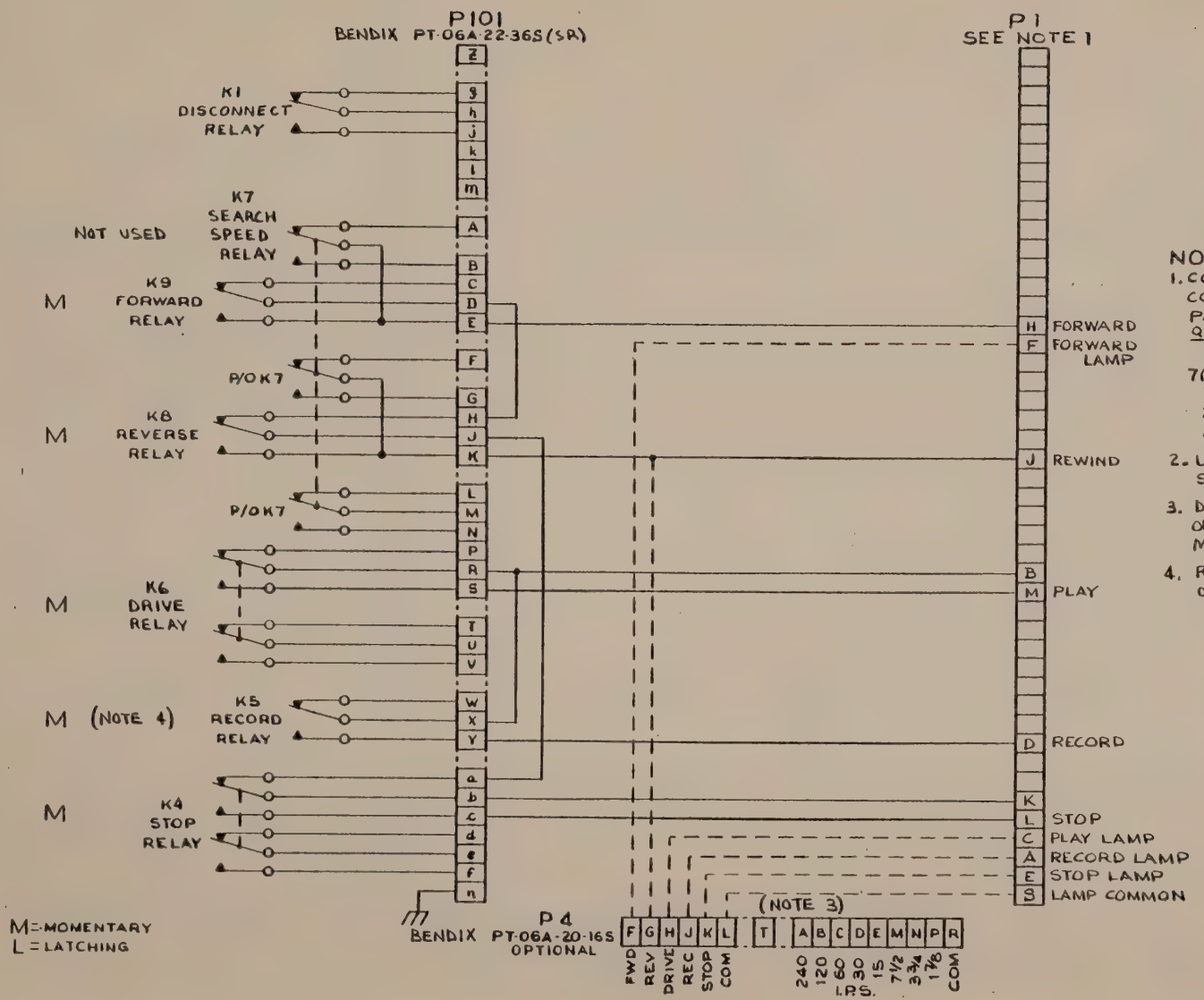
1. Slide shield braid, vinyl tubing, clamp, bushing, cover, spacer, RFI gasket and hood over the wire bundle in the order shown above.
2. Connect pins to appropriate wires and insert pins into the connector block. Crimp type pin connections are recommended for greater reliability and ease of fabrication. Crimp pins and assembly tools are listed in the parts list.
3. Slide hood over connector block and sandwich RFI gasket between hood and spacer. Connect the spacer to the connector with four (4) 4 - 40 X 3/8 cap screws.
4. Slide cover over the spacer and secure with four (4) flat head screws. DO NOT OVERTIGHTEN!
5. Place braid between bushing as shown, and screw clamp onto cover.
6. Install jackscrews as shown.

CONNECTOR ASSEMBLY

INTERFACE CABLE TO MINCOM 110 #041335-7-42 (Sheet 2 of 2)



INTERFACE CABLE TO MINCOM G100 #041335-7-39



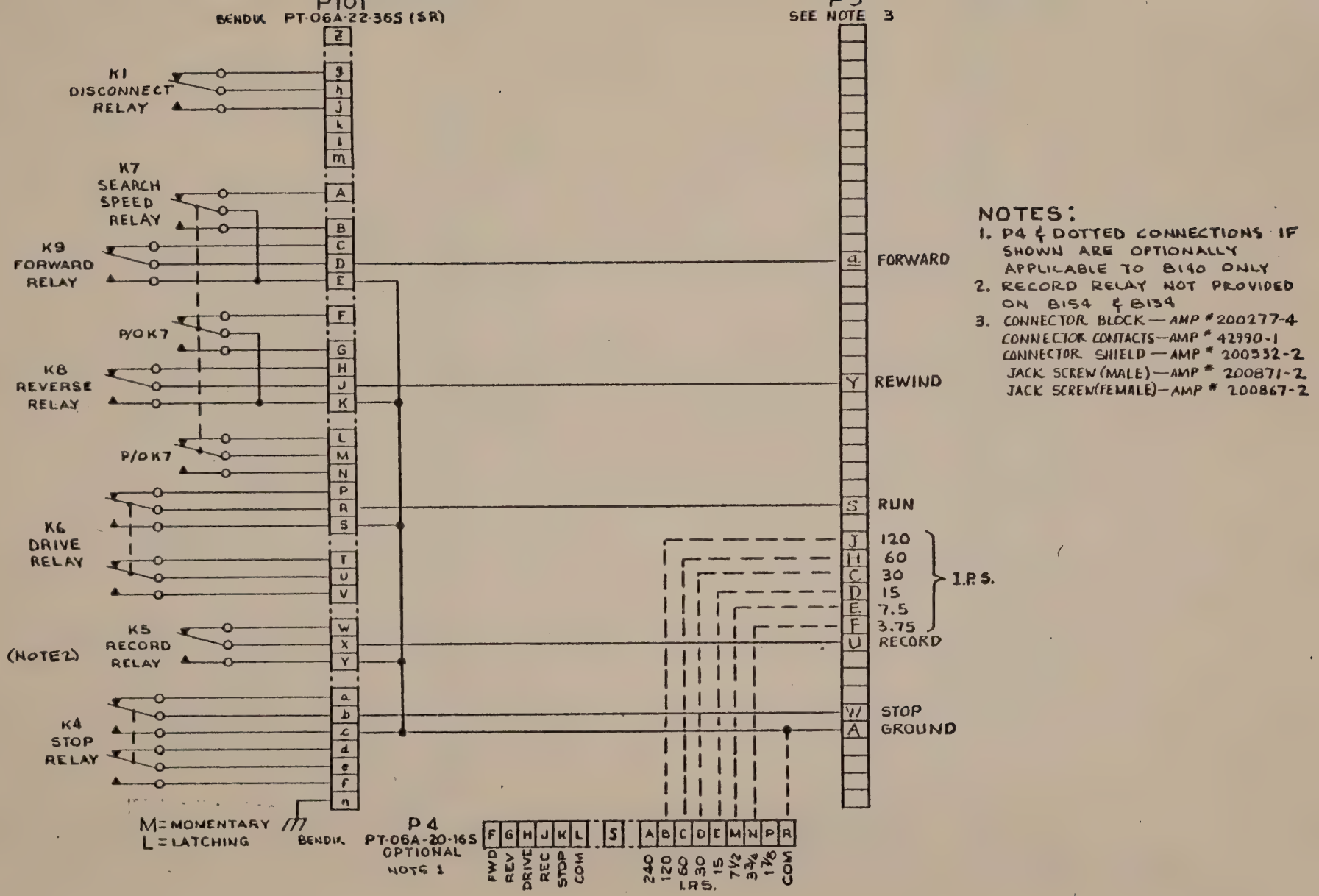
NOTES:

1. CONNECTOR P1, AMP SERIES M CONSISTING OF THE FOLLOWING PARTS:

QTY	AMP PART Nº	DESCRIPTION
1	201359-3	SHELL, 26 POS.
7(12)	42980-1-LP	PIN - CONTACT
1	201229-1	CLAMP, CABLE
2	200389-4	PIN GUIDE
2	201924-1	CLIP, SPRING

2. USE MINIMUM STOP DELAY SETTING.
3. DOTTED CONNECTIONS ARE OPTIONALLY APPLICABLE TO M8140 ONLY.
4. RECORD RELAY K5 NOT PROVIDED ON M8134 & M8154.

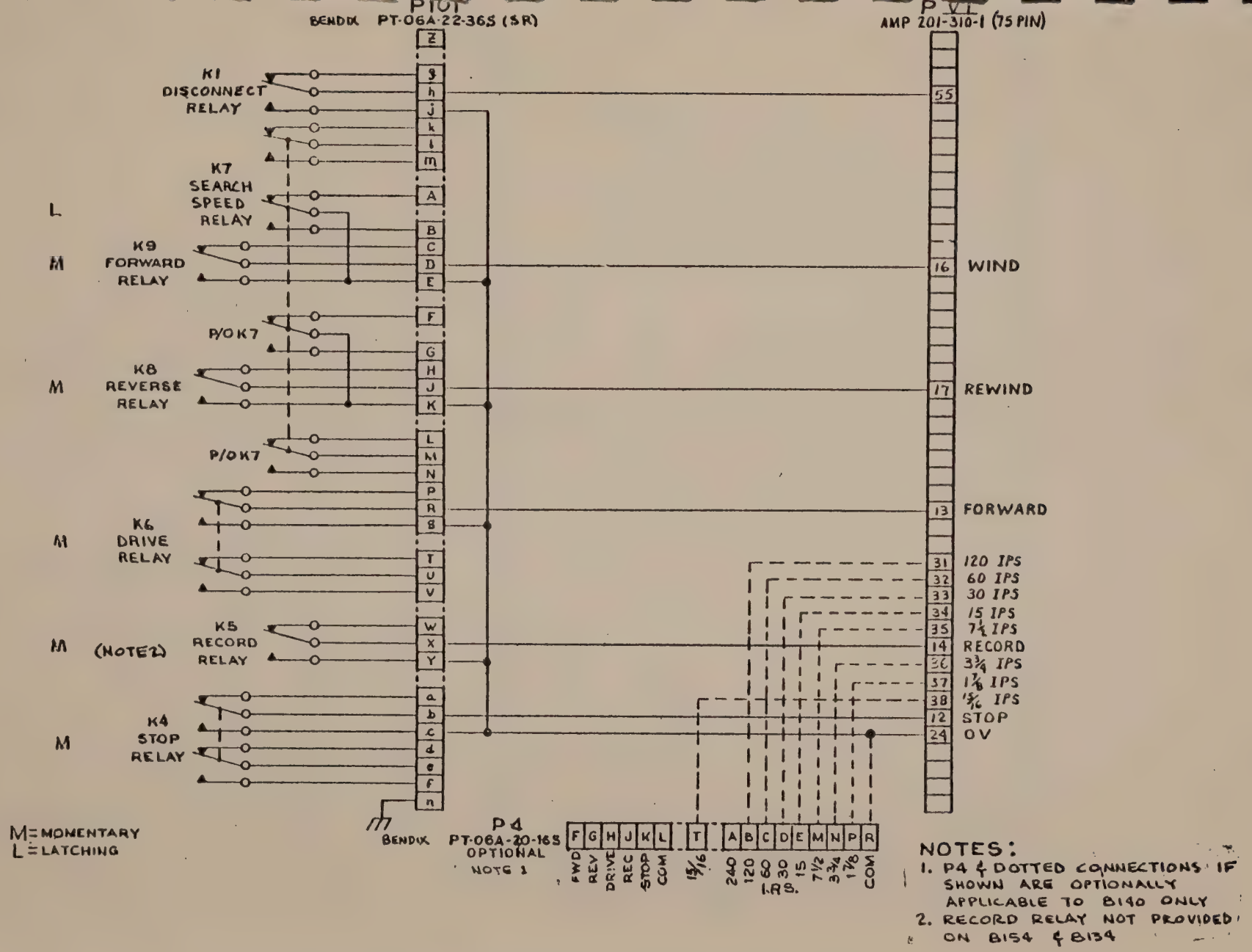
INTERFACE CABLE TO MINCOM PAR410 #031679-7-1 REV A



NOTES:

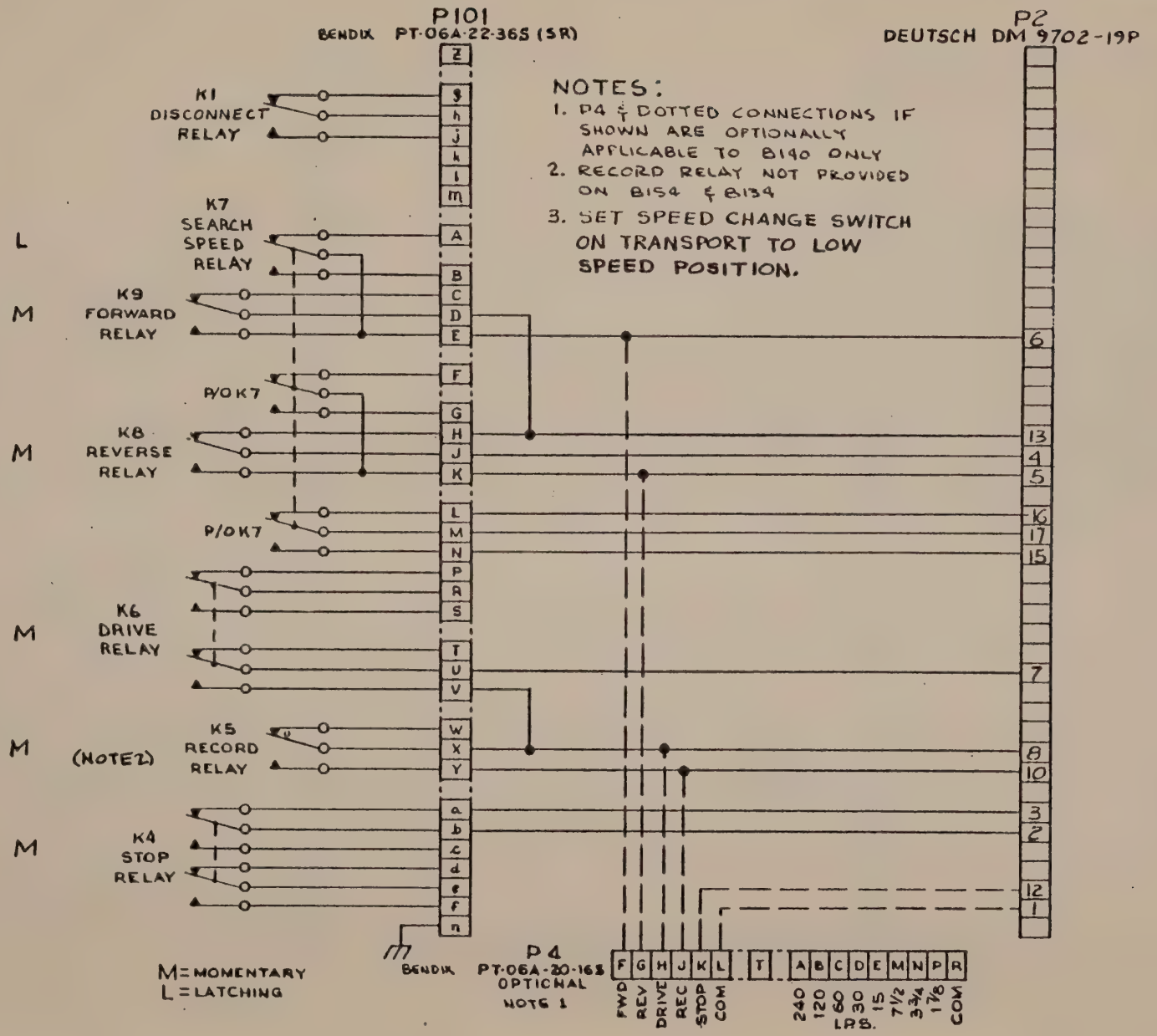
1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134
3. CONNECTOR BLOCK — AMP # 200277-4
   CONNECTOR CONTACTS — AMP # 42990-1
   CONNECTOR SHIELD — AMP # 200532-2
   JACK SCREW (MALE) — AMP # 200871-2
   JACK SCREW (FEMALE) — AMP # 200867-2

INTERFACE CABLE TO MINCOM TICOR III #041335-7-87 REV A

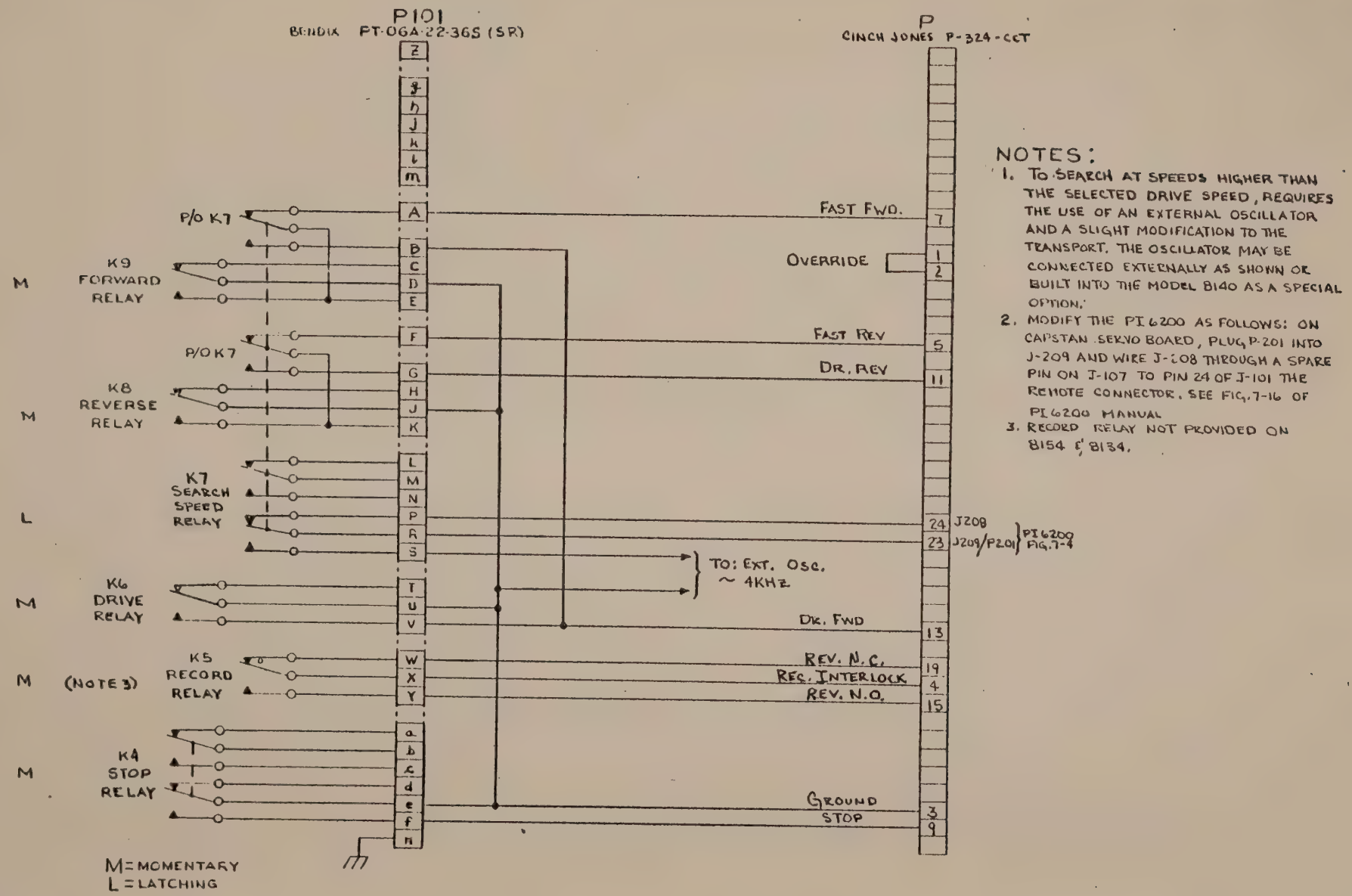


NOTES:
1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134

INTERFACE CABLE TO PHILLIPS EL-1016 #041335-7-48



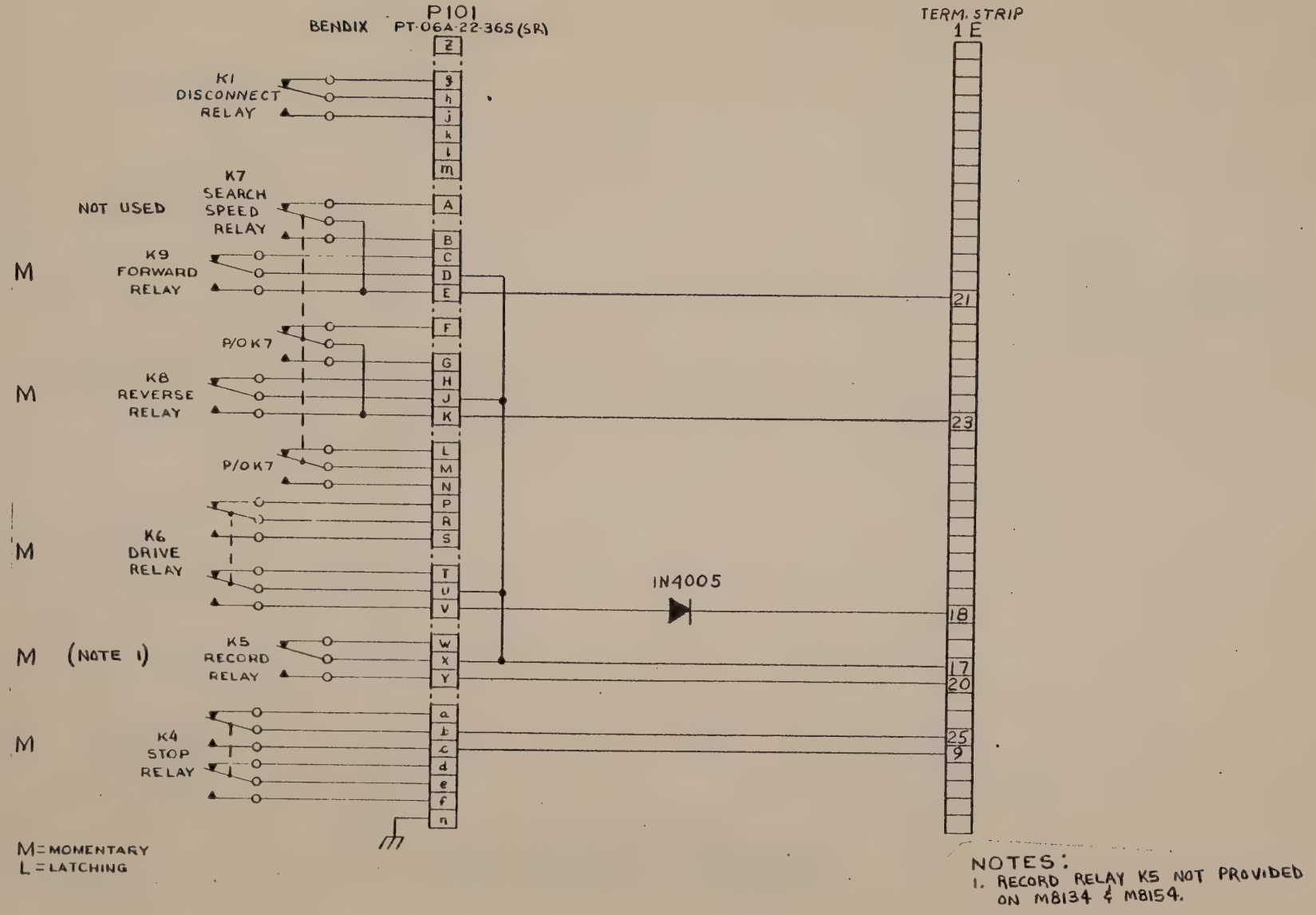
INTERFACE CABLE TO PRECISION INSTRUMENT 214 #041335-7-41



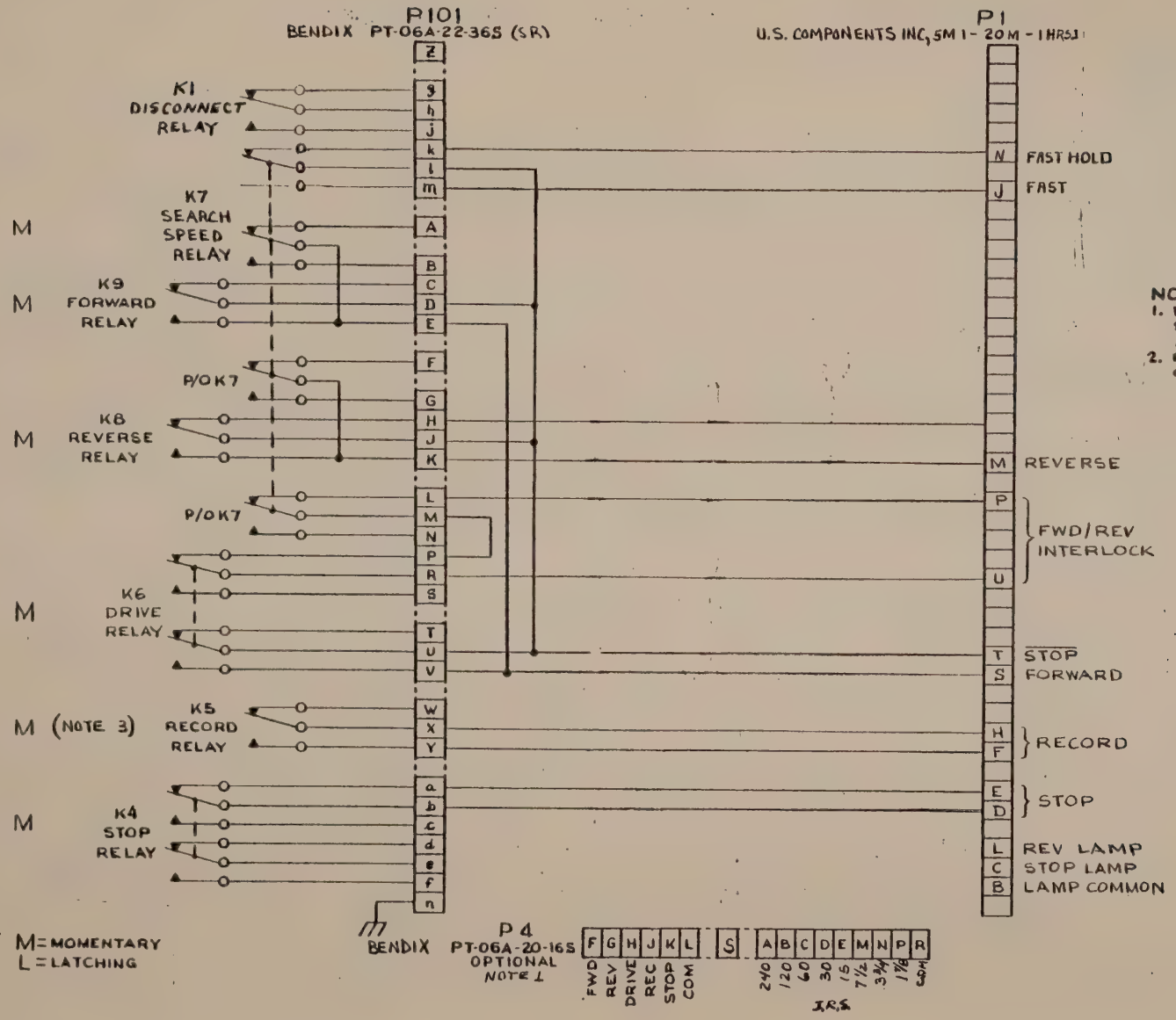
NOTES:

1. TO SEARCH AT SPEEDS HIGHER THAN THE SELECTED DRIVE SPEED, REQUIRES THE USE OF AN EXTERNAL OSCILLATOR AND A SLIGHT MODIFICATION TO THE TRANSPORT. THE OSCILLATOR MAY BE CONNECTED EXTERNALLY AS SHOWN OR BUILT INTO THE MODEL 8140 AS A SPECIAL OPTION.
2. MODIFY THE PI 6200 AS FOLLOWS: ON CAPSTAN SERVO BOARD, PLUG P-201 INTO J-209 AND WIRE J-208 THROUGH A SPARE PIN ON J-107 TO PIN 24 OF J-101 THE REMOTE CONNECTOR. SEE FIG. 7-16 OF PI 6200 MANUAL
3. RECORD RELAY NOT PROVIDED ON 8154 & 8134.

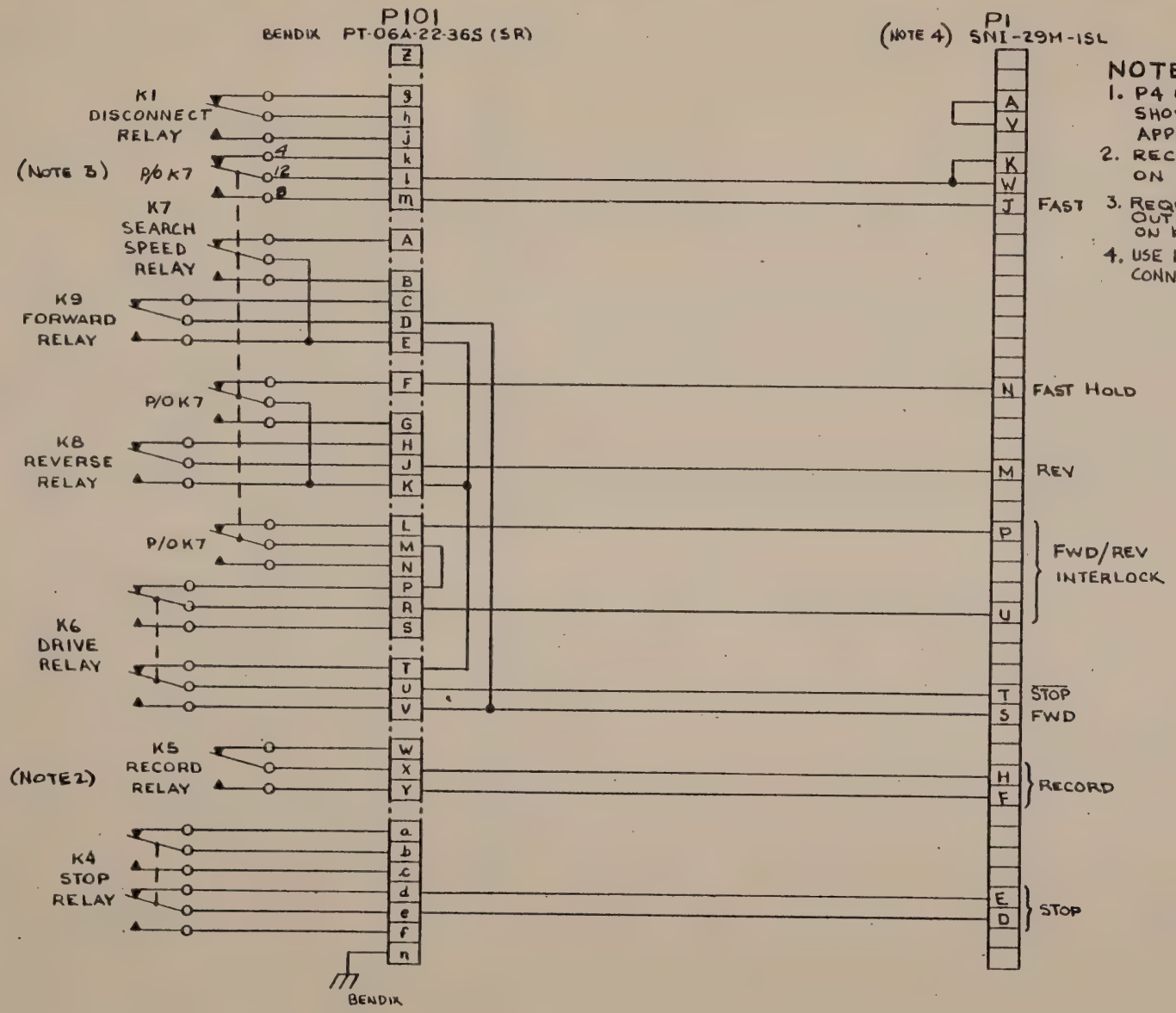
INTERFACE CABLE TO PRECISION INSTRUMENT 6200 #041335-7-33



INTERFACE CABLE TO SANGAMO 472RB #031316-7-1 REV B



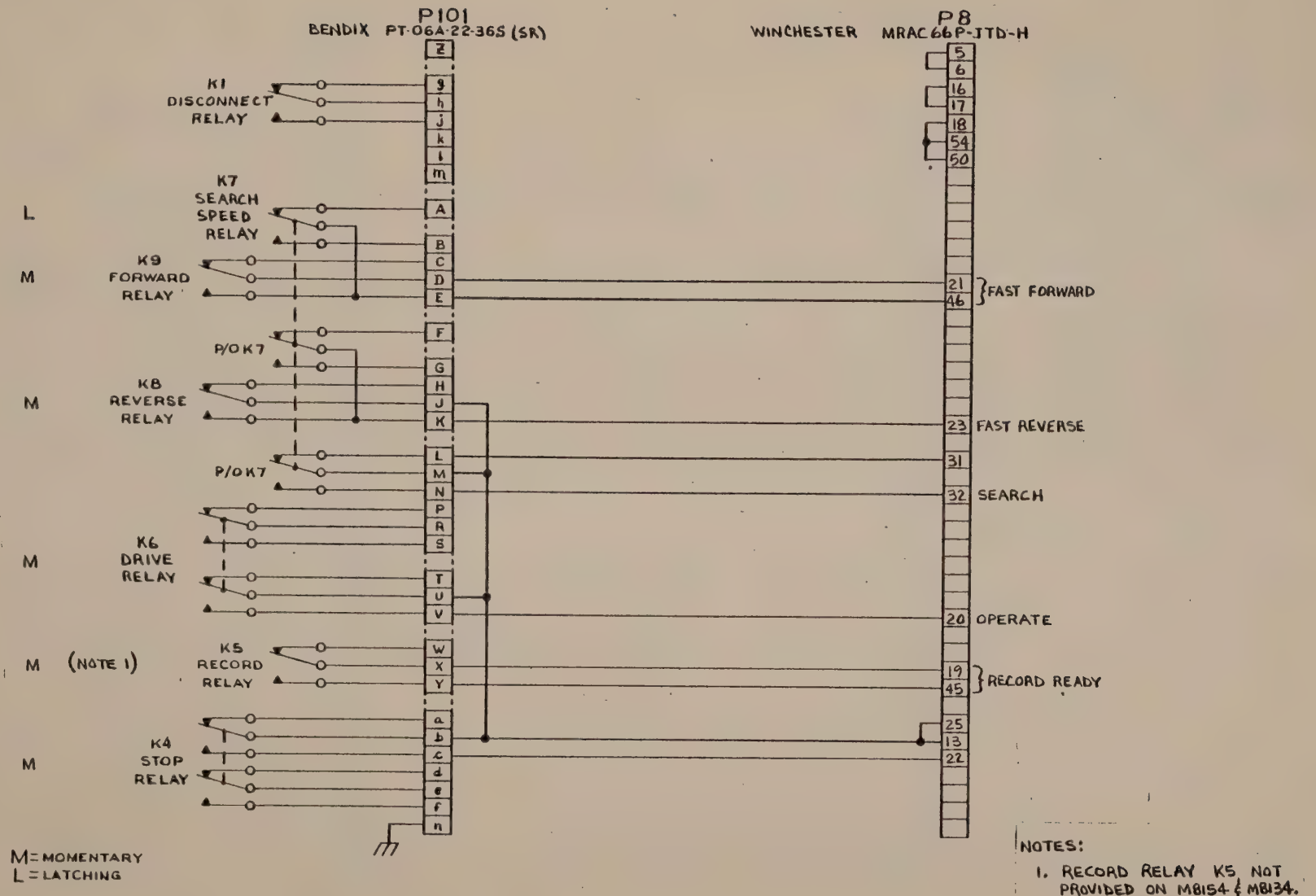
INTERFACE CABLE TO SANGAMO 3500 SERIES #031173-7-1 REV C



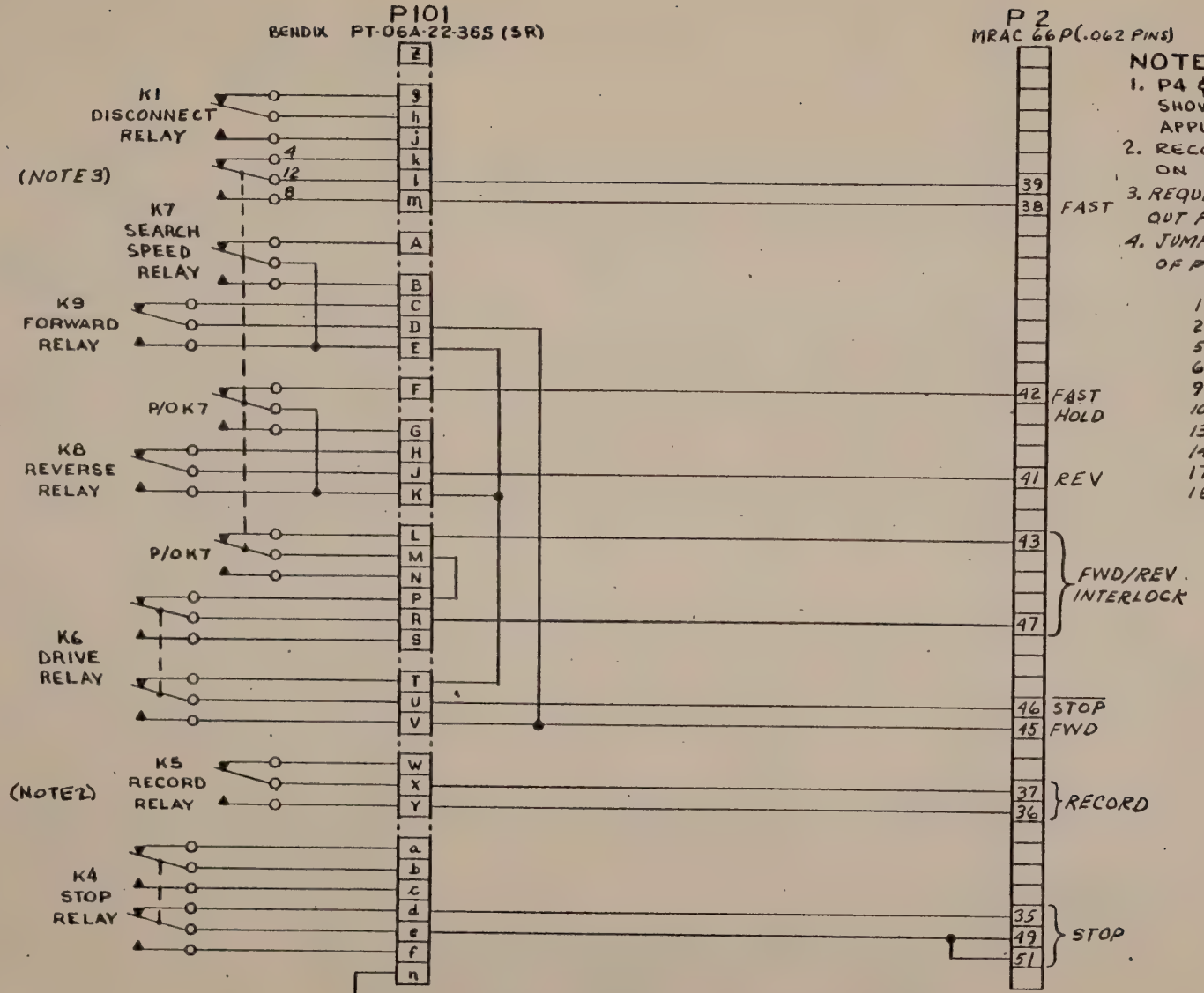
NOTES:

1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134
3. REQUIRES MODIFICATION TO BRING OUT FOURTH SET OF CONTACTS ON K7.
4. USE HOOD SMI-29-HIRSL WITH P1 CONNECTOR.

INTERFACE CABLE TO SANGAMO 3600 #041335-7-31 REV A



INTERFACE CABLE TO SANGAMO 4700 SERIES #031528-7-1 REV A

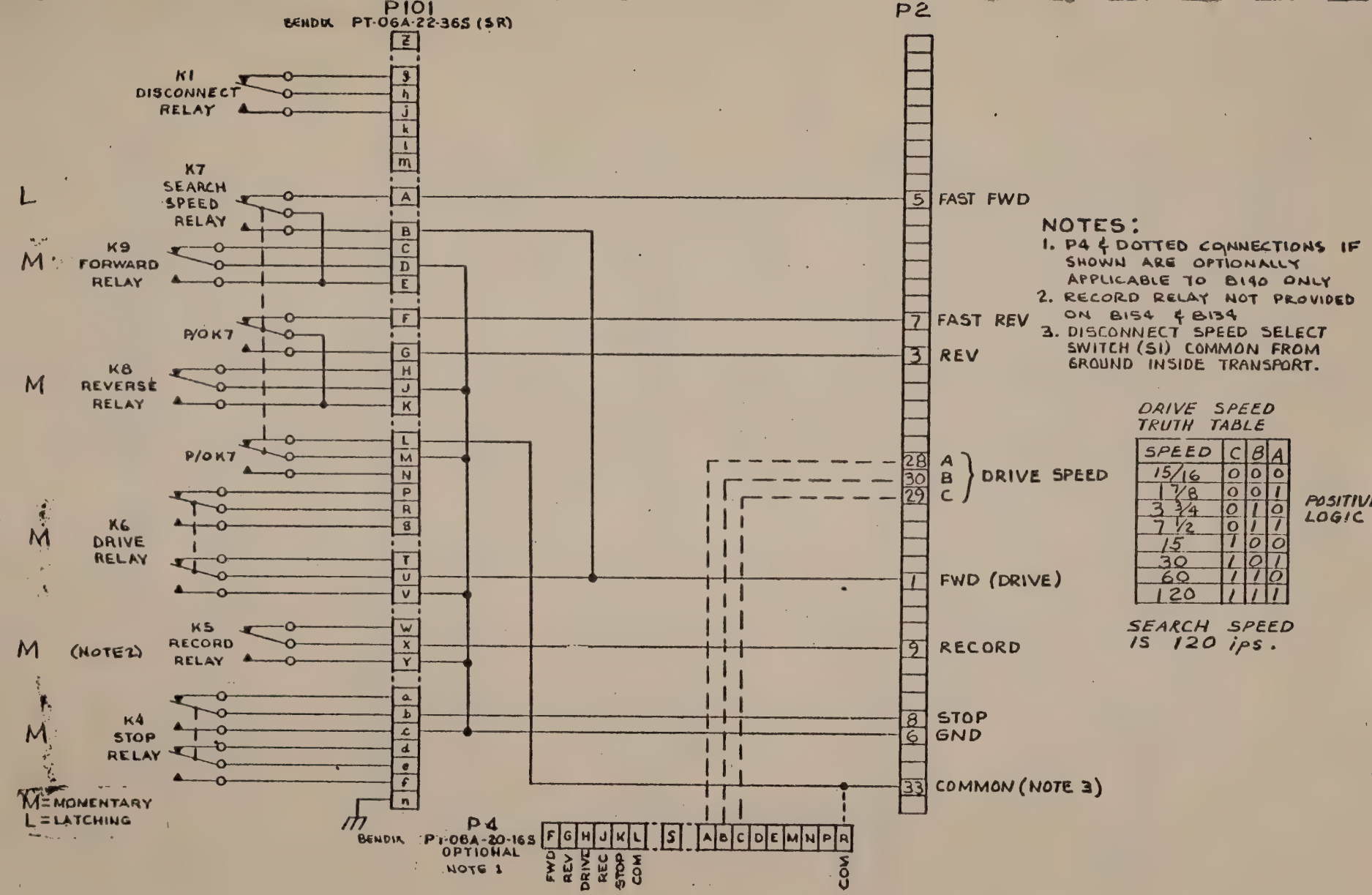


NOTES:

1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134
3. REQUIRES MODIFICATION TO BRING OUT FOURTH SET OF CONTACTS ON K7
4. JUMPER THE FOLLOWING PAIRS OF PINS ON P2:

1-3	21-23
2-4	22-24
5-7	25-27
6-8	26-28
9-11	50-52
10-12	55-56
13-15	58-59
14-16	61-62
17-19	
18-20	

INTERFACE CABLE TO SANGAMO 4900 #041335-7-34



NOTES:

1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO B140 ONLY
2. RECORD RELAY NOT PROVIDED ON B154 & B134
3. DISCONNECT SPEED SELECT SWITCH (S1) COMMON FROM GROUND INSIDE TRANSPORT.

DRIVE SPEED TRUTH TABLE

SPEED	C	B	A
15/16	0	0	0
1 7/8	0	0	1
3 3/4	0	1	0
7 1/2	0	1	1
15	1	0	0
30	1	0	1
60	1	1	0
120	1	1	1

POSITIVE LOGIC

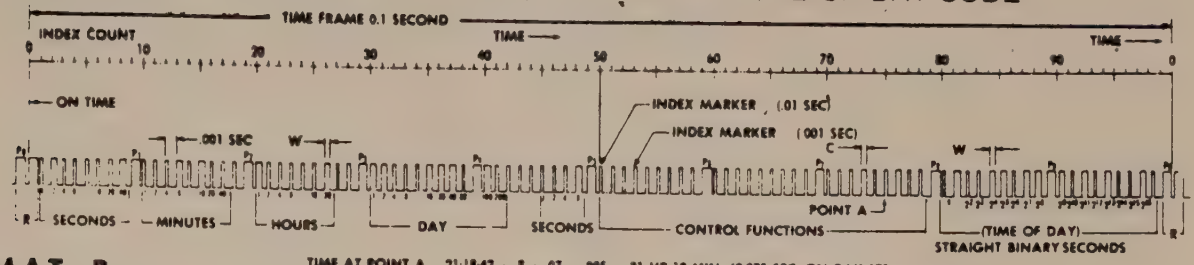
SEARCH SPEED IS 120 ips.

INTERFACE CABLE TO SANGAMO (SABRE VI) # 041335-7-93 REV A

IRIG TIME CODE FORMATS

FORMAT A

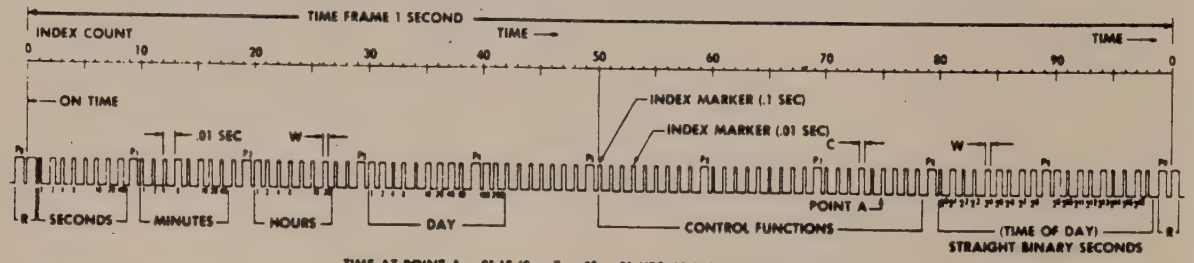
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A 21:18:42 - .8 - .07 - .005 21 HR. 18 MIN. 42.875 SEC ON DAY 173

FORMAT B

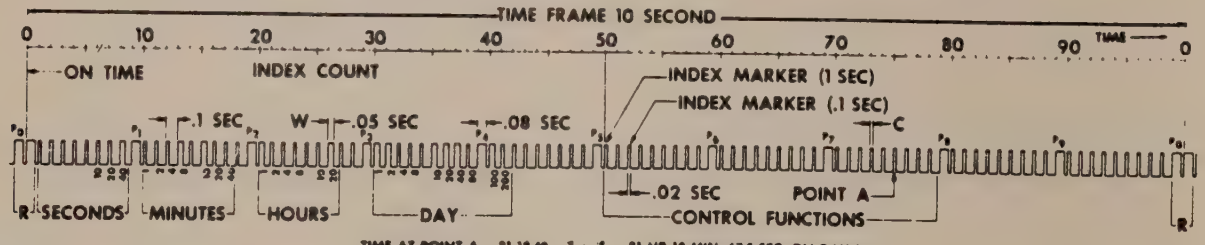
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A - 21:18:42 - .7 - .05 - 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

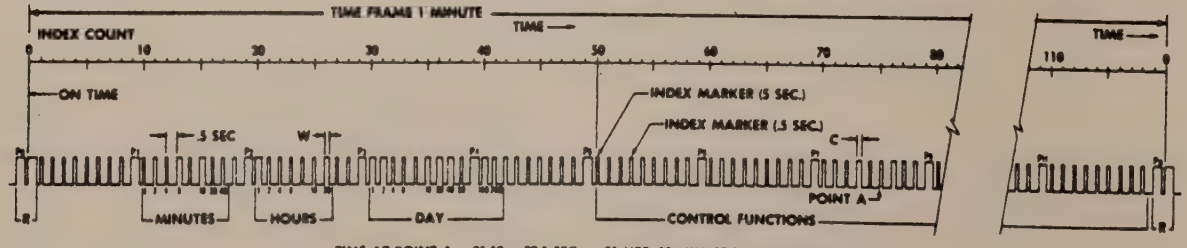
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A - 21:18:40 - .7 - .5 - 21 HR. 18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

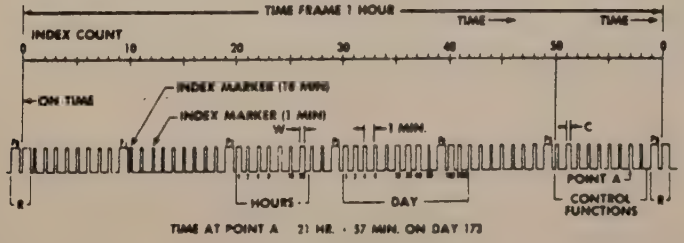
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



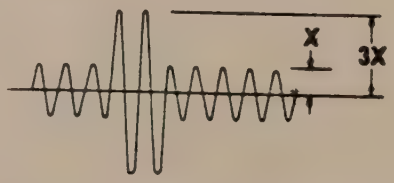
TIME AT POINT A - 21:18 + 37.5 SEC. - 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE

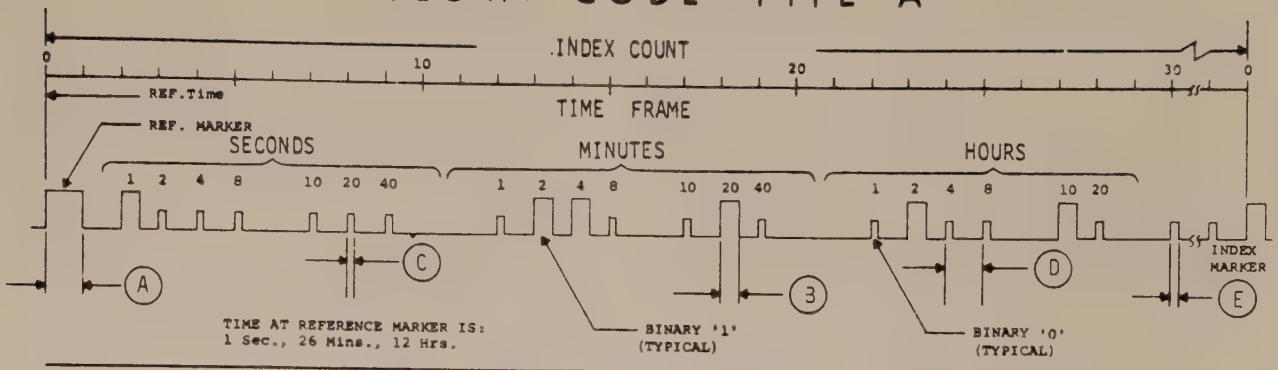


TIME AT POINT A 21 HR. - 37 MIN. ON DAY 173



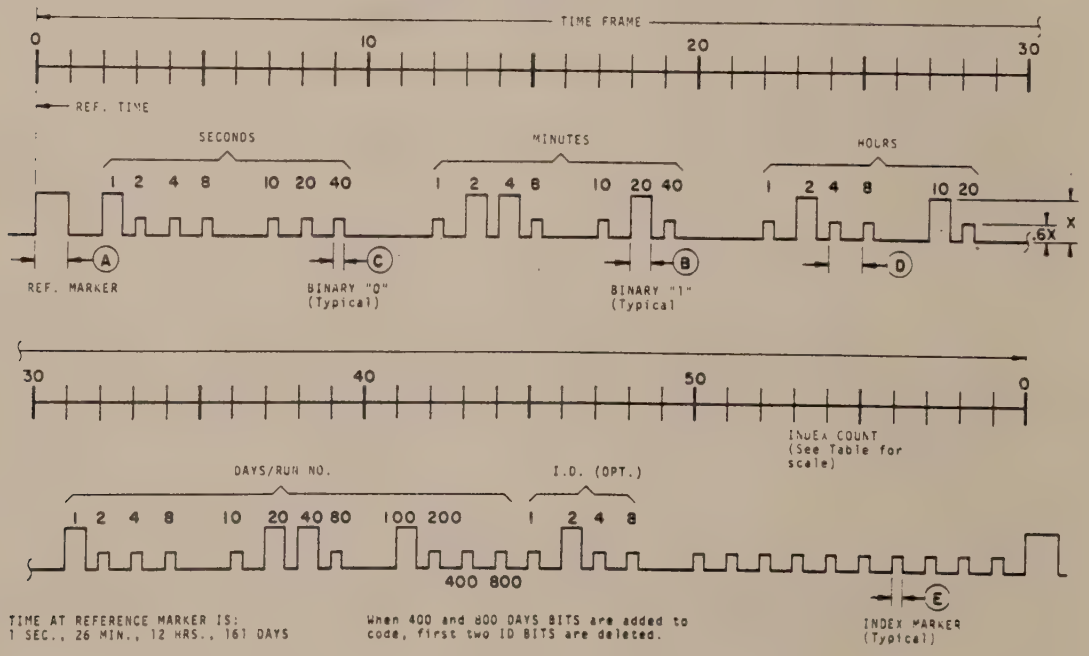
TYPICAL MODULATED SIGNAL

SLOW CODE - TYPE 'A'



	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec.	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs.	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs.	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs.	1 Sec.	1 Sec.	500 ms	200 ms	200 ms	30
5	1/2 pps	60 Secs.	2 Secs.	2 Secs.	1 Sec.	400 ms	400 ms	30
6	1/10 pps	5 Mins.	10 Secs.	10 Secs.	5 Secs.	2 Secs.	2 Secs.	30
7	1/20 pps	10 Mins.	20 Secs.	20 Secs.	10 Secs.	4 Secs.	4 Secs.	30
8	1 ppm	30 Mins.	1 Min.	1 Min.	30 Secs.	12 Secs.	12 Secs.	30
9	1/2 ppm	60 Mins.	2 Mins.	2 Mins.	1 Min.	24 Secs.	24 Secs.	30

SLOW CODE -- TYPE "B"

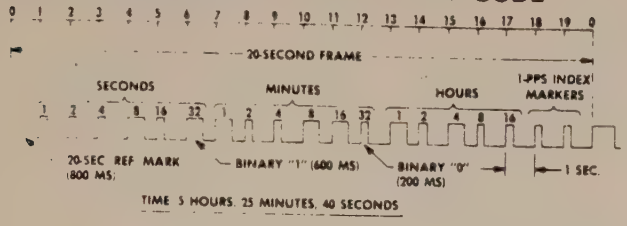


	Pulse Rate	Time Frame	D-Period	A-Width	B-Width	C-Width	E-Width	Number of Pulses in Time Frame
1.	50	1 SEC	20 ms	20 ms	10 ms	4 ms	4 ms	50
2.	10	5 SEC	100 ms	100 ms	50 ms	20 ms	20 ms	50
3.	5	10 SEC	200 ms	200 ms	100 ms	40 ms	40 ms	50
4.	2	30 SEC	1/2 SEC	1/2 SEC	250 ms	100 ms	100 ms	60
5.	1	60 SEC	1 SEC	1 SEC	1/2 SEC	200 ms	200 ms	60
6	1/2	5 MIN	5 SEC	5 SEC	2-1/2 SEC	1 SEC	1 SEC	60
7.	1/10	10 MIN	10 SEC	10 SEC	5 SEC	2 SEC	2 SEC	60
8	2 ppm	30 MIN	30 SEC	30 SEC	10 SEC	6 SEC	6 SEC	60
9	1 ppm	60 MIN	60 SEC	60 SEC	30 SEC	12 SEC	12 SEC	60

AMR TIME CODE FORMATS

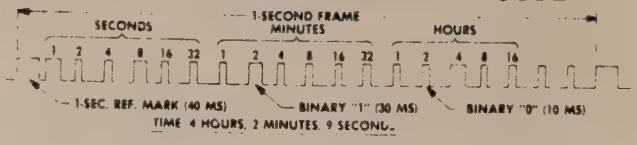
ATLANTIC MISSILE RANGE NO. B1

17-BIT, 1-PPS, BINARY TIME-OF-DAY CODE



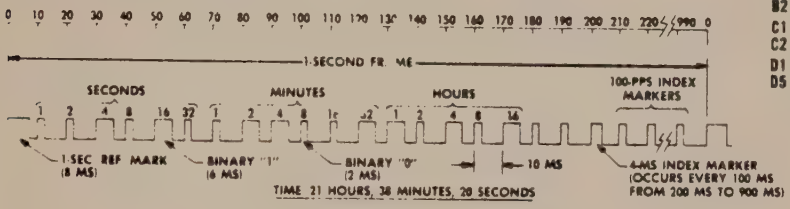
ATLANTIC MISSILE RANGE NO. C1

17-BIT, 20-PPS, BINARY TIME-OF-DAY CODE



ATLANTIC MISSILE RANGE NO. D1

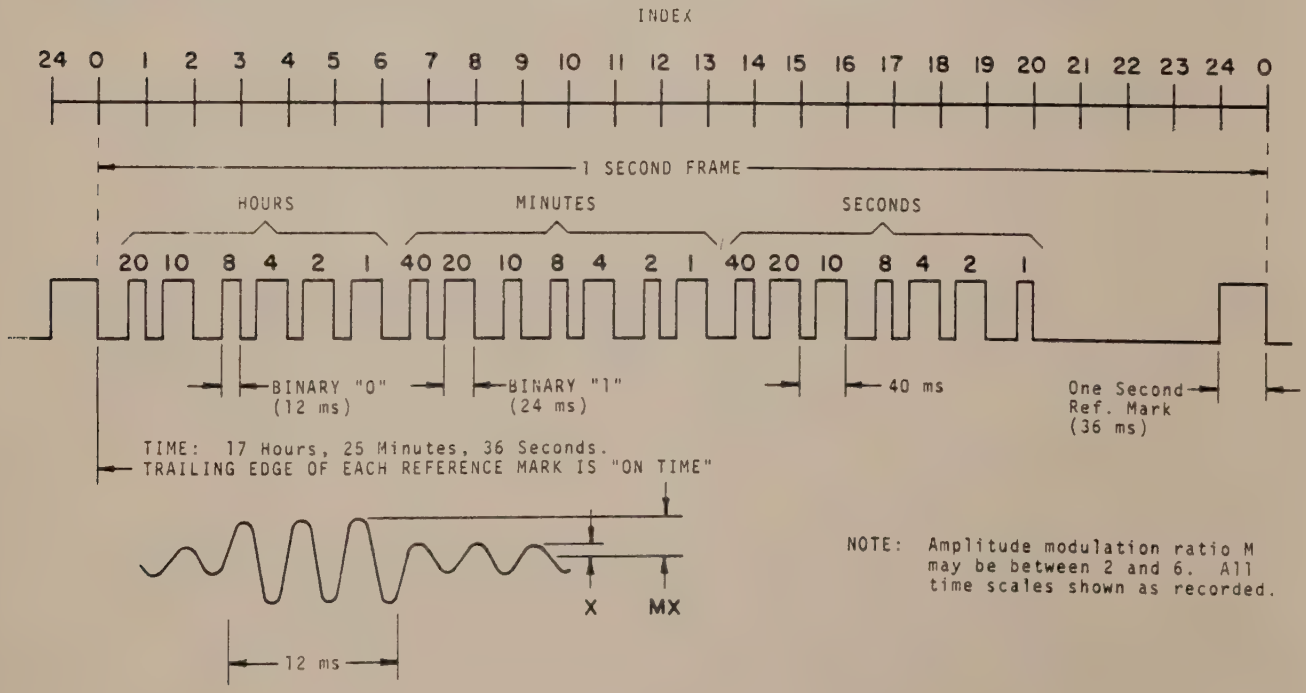
17-BIT, 100-PPS, BINARY TIME-OF-DAY CODE



AMR SIGNAL DESIGNATIONS

AMR NO.	17-BIT, 24-HOUR BINARY CODE
B1	1 PPS (pulse width)
B2	1 PPS (modulated)
C1	20 PPS (pulse width)
C2	20 PPS (modulated)
D1	100 PPS (pulse width)
D5	100 PPS (modulated)

XR 3 TIME CODE FORMAT



NOTE: Amplitude modulation ratio M may be between 2 and 6. All time scales shown as recorded.

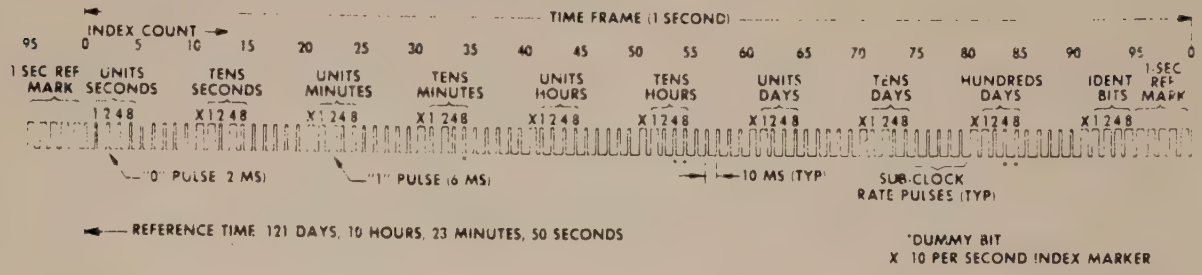
TYPICAL MODULATED CODE ELEMENT "ZERO" (250 Hz Carrier)

For 1 kHz carrier large amplitude cycles number 12, 24, and 36

NASA TIME CODE FORMATS

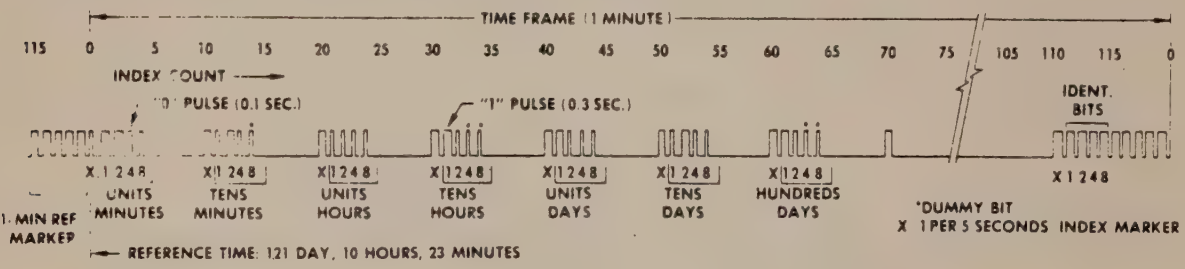
36-BIT, 100-PPS CODE (1000-CPS CARRIER)

SHOWING SUB-CLOCK RATE PULSES



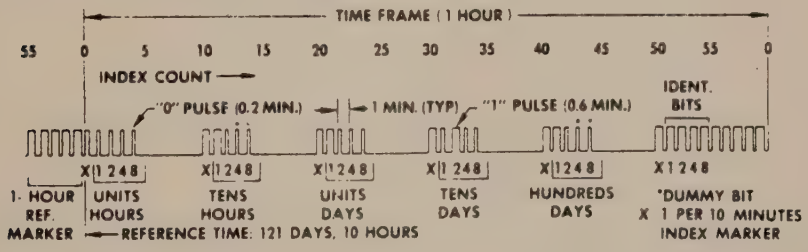
28-BIT, 2-PPS CODE (100-CPS CARRIER)

SUB CLOCK RATE PULSES INHIBITED

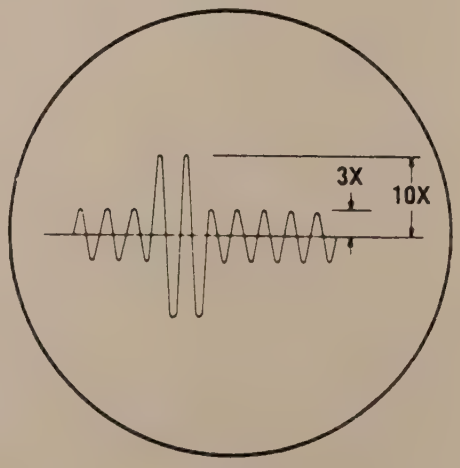


20-BIT, 1-PPM CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED



Insertion of sub-clock rate pulses is controlled for each format by individual control switches.



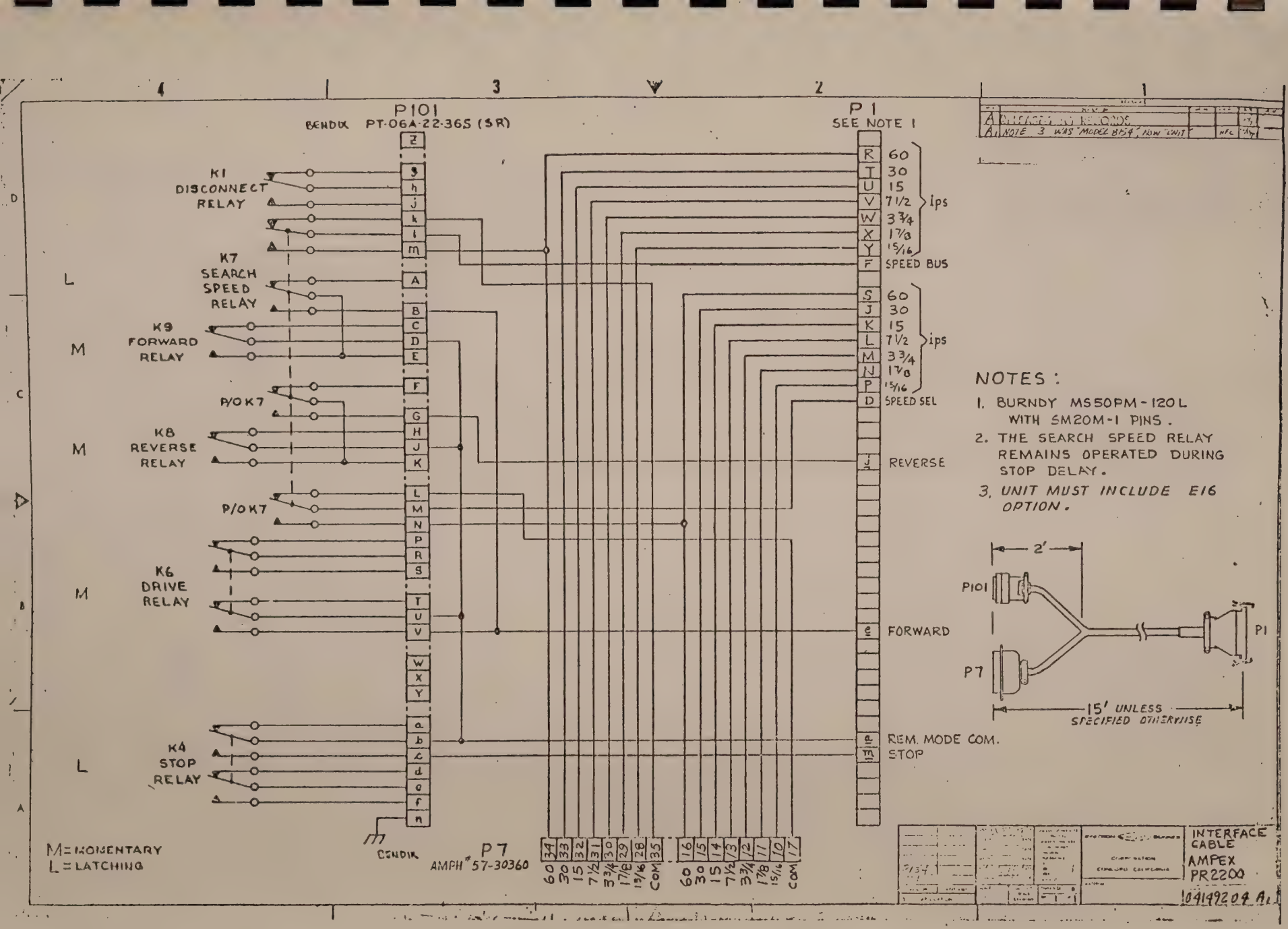
TYPICAL MODULATED SIGNAL

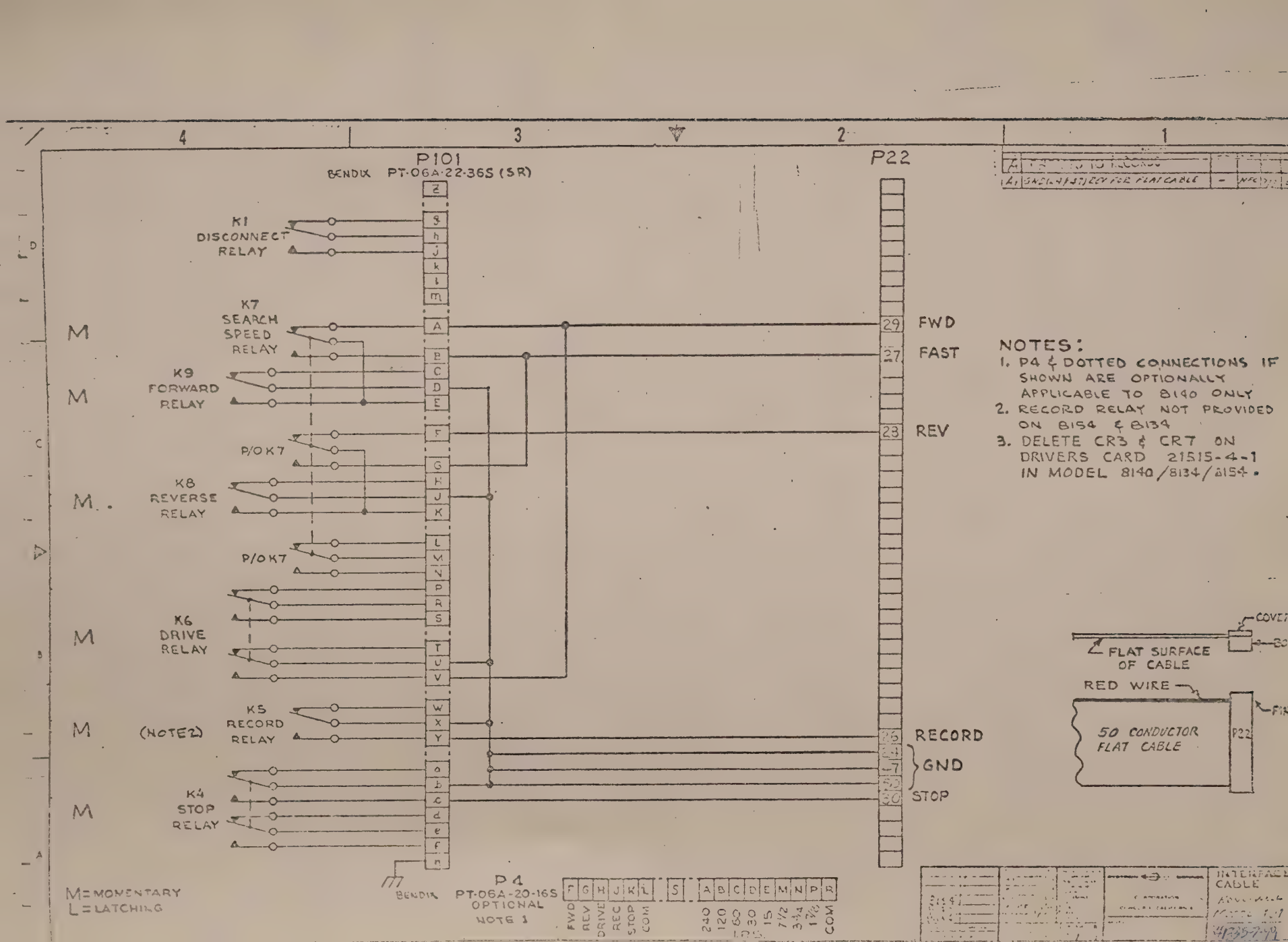
PARTS LIST

INTERFACE CABLE AMPEX PR2200

#04149204

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	04149204
	#24 Awg. Insul. Wire A/R Sleeving A/R	
P1	Connector, 360 Position (Amphenol 57-30360) Contact Pins (Reel) Burndy SM20M-1 Contact Pins (Loose) Burndy RM20M-12	
P7	Connector, 36 Position (Amphenol 57-30360)	101158
P101	Connector, 36 Position (Bendix PT06A-22-36S(SR)	101213
	Crimp Tool (Hand) Burndy N8ND Die Set (SM20M-1) Burndy N20RT-29 Die Set (RM20M-12) Burndy N24RT-30 Extraction Tool (SM20M-1) Burndy RX20-25 Extraction Tool (RM20M-12) Burndy RX16-D11	


P101
BENDIX PT-06A-22-36S (SR)
P1
SEE NOTE 1
K1 DISCONNECT RELAY
K7 SEARCH SPEED RELAY
K9 FORWARD RELAY
P/O K7
K8 REVERSE RELAY
P/O K7
K6 DRIVE RELAY
K4 STOP RELAY
M = MOMENTARY
L = LATCHING
CENDIX
P7
AMPH* 57-30360
60
30
15
7 1/2
3 3/4
1 7/8
15/16
SPEED BUS
SPEED SEL
REVERSE
FORWARD
REM. MODE COM.
STOP
ips
NOTES:
1. BURNDY MS50PM-120L WITH SM20M-1 PINS.
2. THE SEARCH SPEED RELAY REMAINS OPERATED DURING STOP DELAY.
3. UNIT MUST INCLUDE E16 OPTION.
2'
P101
P1
P7
15' UNLESS SPECIFIED OTHERWISE
INTERFACE CABLE
AMPEX
PR2200
104192 04 A1


P101
BENDIX PT-06A-22-36S (SR)
P22
K1
DISCONNECT
RELAY
K7
SEARCH
SPEED
RELAY
K9
FORWARD
RELAY
P/O K7
K8
REVERSE
RELAY
P/O K7
K6
DRIVE
RELAY
K5
RECORD
RELAY
(NOTE 2)
K4
STOP
RELAY
M
FWD
FAST
REV
RECORD
GND
STOP
NOTES:
1. P4 & DOTTED CONNECTIONS IF SHOWN ARE OPTIONALLY APPLICABLE TO 8140 ONLY
2. RECORD RELAY NOT PROVIDED ON 8154 & 8134
3. DELETE CR3 & CR7 ON DRIVERS CARD 21515-4-1 IN MODEL 8140/8134/8154.
FLAT SURFACE OF CABLE
RED WIRE
50 CONDUCTOR FLAT CABLE
P22
P4
PT-06A-20-16S
OPTIONAL
NOTE 1
FWD
REV
DRIVE
REC
STOP
COM
240
120
60
30
15
7½
3.44
1.72
COM
M=MOMENTARY
L=LATCHING

PARTS LIST
INTERFACE CABLE HONEYWELL MODEL 101 #41335-7-99

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic/Assembly	041335-7-99
	Assembly, Drivers	021515-4-7
P22	Connector, Flat 50 Pin (3M #3425-000)	
P101	Connector (Bendix PT06A-22-36S [SR])	101213
	Bushing, #10	100947
	Plug, Cable Clamp	061111
	Cable, Flat 50 Conductor (3M #3365, 28 Awg. Stranded)	
	DELETE	
	Assembly, Drivers	021515-4-1

- -

PARTS LIST
DRIVERS #021515-8-7 REV A_1

REFERENCE	DESCRIPTION	SD PART NO.
	ADD	
CR14	Diode 1N4151	100385
	DELETE	
CR3	Diode In4151	
CR7	Same as CR3	

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